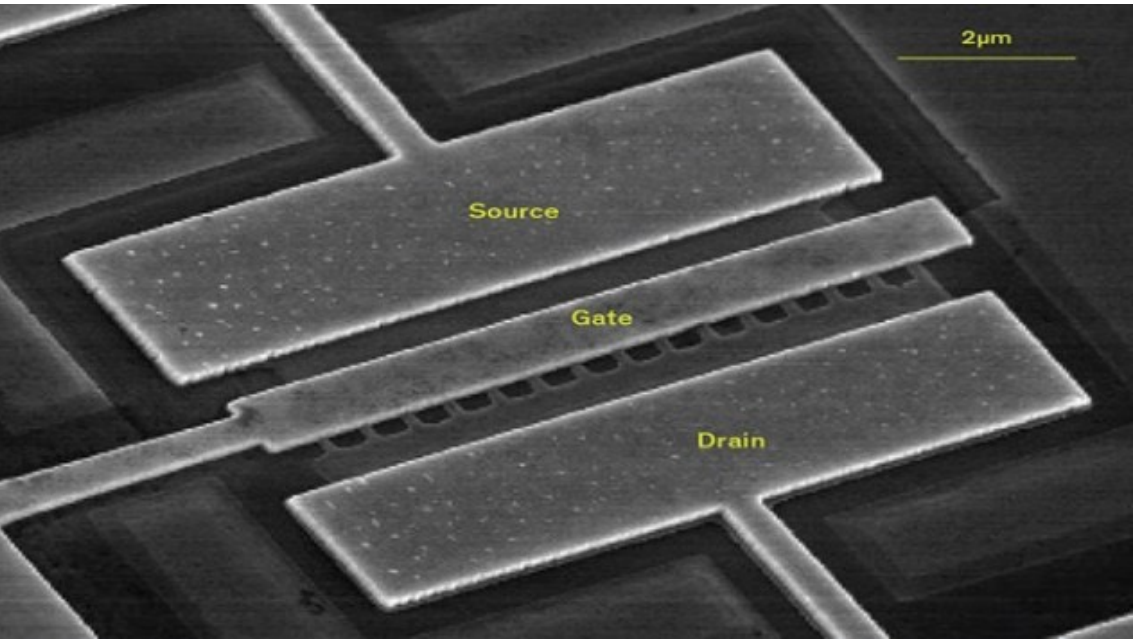
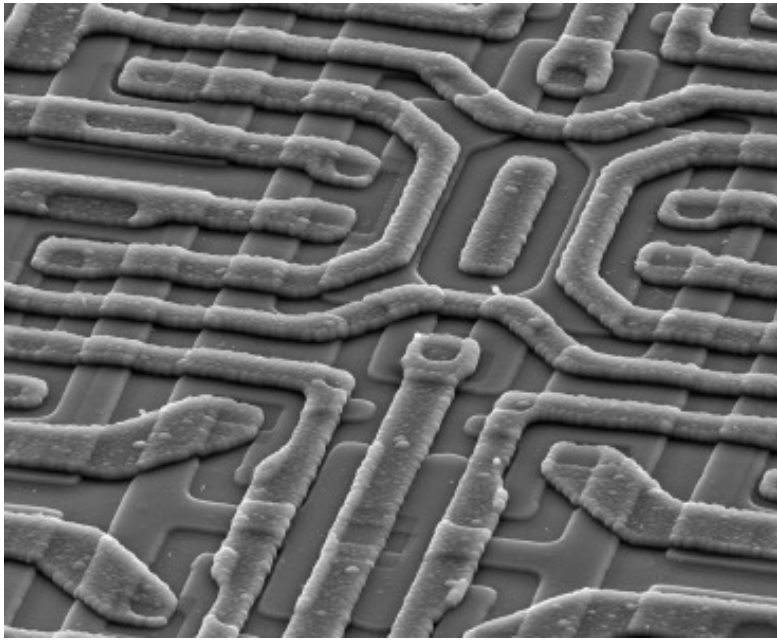
PHYS127AL Lecture 9

David Stuart, UC Santa Barbara

Field effect transistors (FETs)





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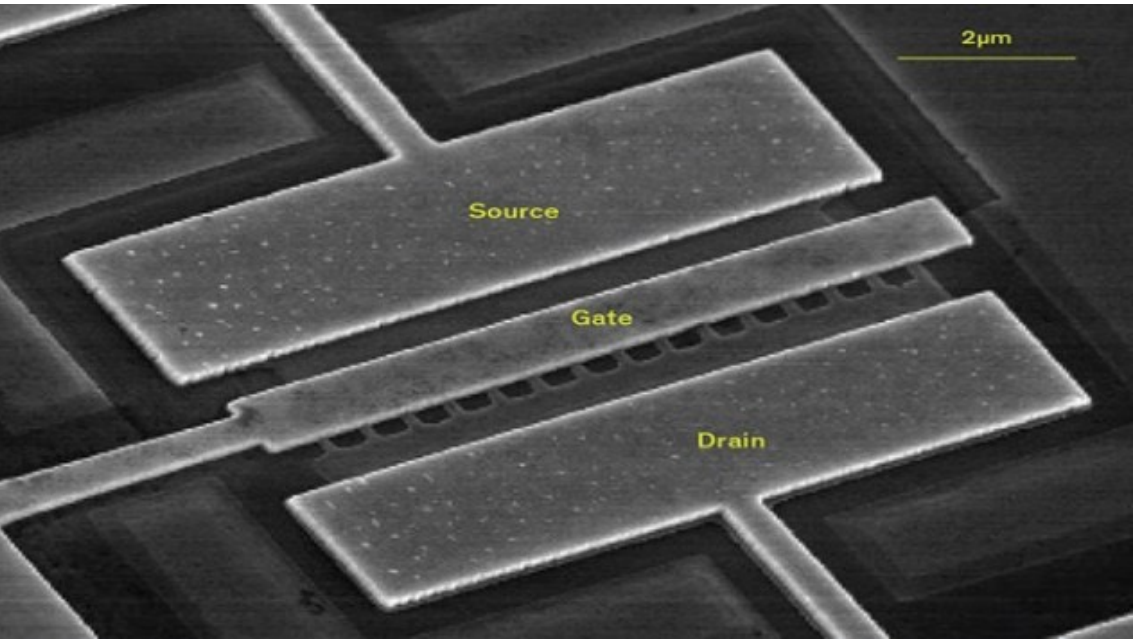
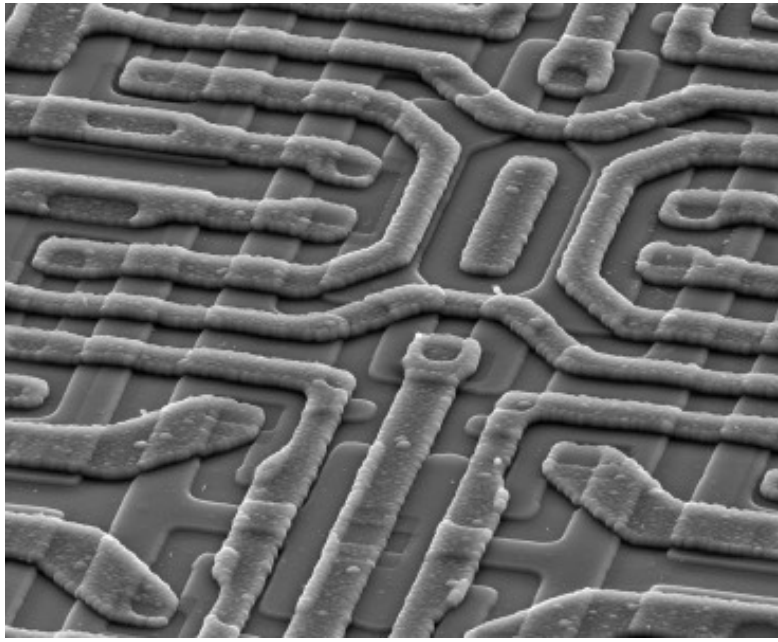




How many of you have heard of "CMOS" before?

Review: More complete transistor model

We used simplified (0th and 1st order) models:

1). V_{BE} = 0.6 V or the transistor is off
I.e., $V_B = V_E + 0.6$ V
Once the transistor is on, $\Delta V_B = \Delta V_E$.

$$I_C = I_s \left(e^{V_{BE}/nV_T} - 1 \right)$$

2). $I_C = \beta I_B$.
And by charge conservation
$I_E = I_B + I_C$ so $I_E \cong I_C$

3). $V_{CE} > 0.2$ V

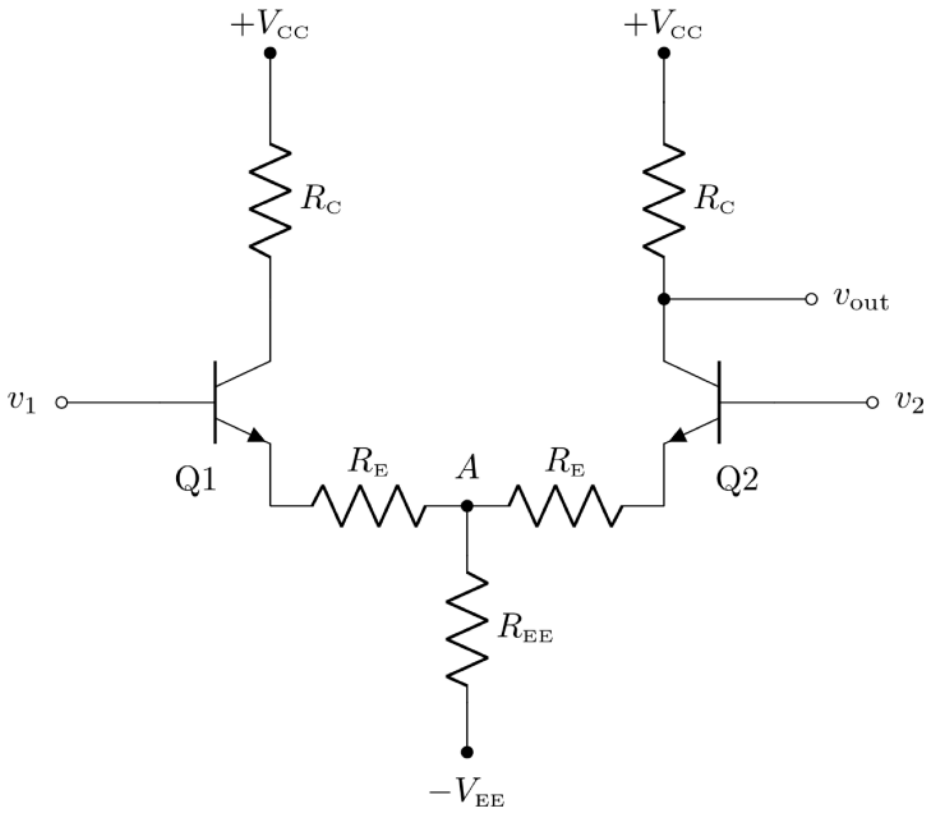
A 2nd order correction incorporates effects from collector voltage differences

$$I_C = I_S \left(e^{V_{BE}/nV_T} - 1 \right) \left(1 + \frac{V_{CE}}{V_{AF}} \right) - I_S \left(e^{V_{BC}/nV_T} - 1 \right) \left(1 + \frac{V_{CE}}{V_{AR}} \right) - \frac{I_S}{\beta_R} \left(e^{V_{BC}/nV_T} - 1 \right)$$

$$I_B = \frac{I_S}{\beta_F} \left(e^{V_{BE}/nV_T} - 1 \right) - \frac{I_S}{\beta_R} \left(e^{V_{BC}/nV_T} - 1 \right).$$

(Ebers–Moll equations with Early correction)

Review: Differential amplifier



Get positive gain by selecting output from $v_2 = -v/2$

Don't need output from other side, but we do need the other side to get the common mode suppression.

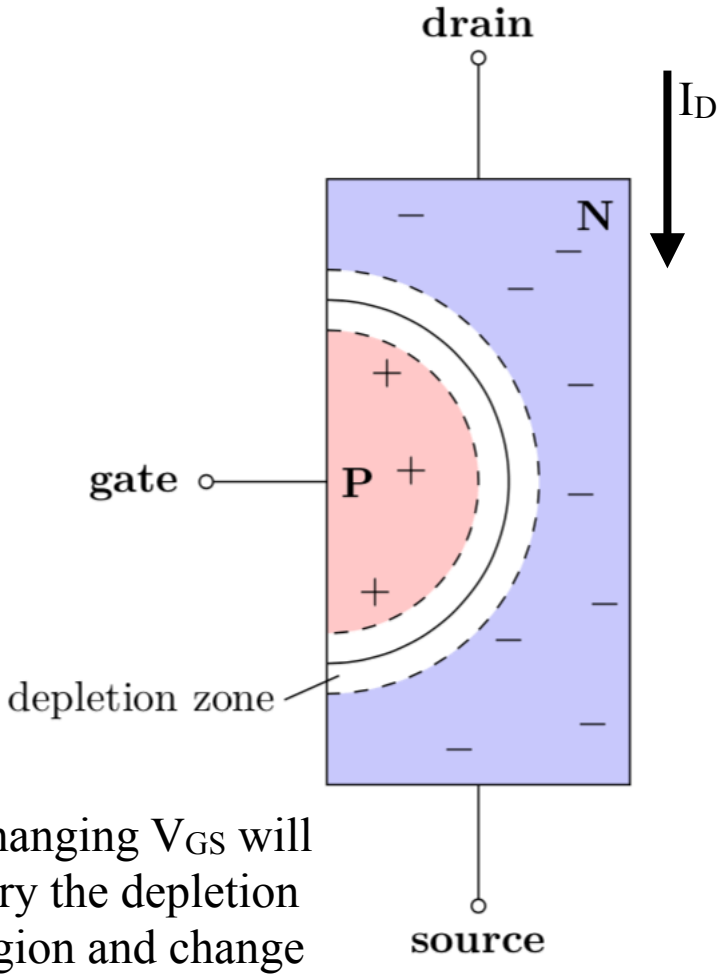
To maximize the CMRR = G_{Diff}/G_{CM} make R_{EE} large.

A current source has infinite impedance.

Common mode gain = $-R_C/(R_E+2R_{EE})$
Differential gain = $R_C/2R_E$

Field effect transistors (FETs)

The NPN and PNP transistors we've discussed so far are called bi-polar junction transistors (BJT). FETs operate under a different mechanism.

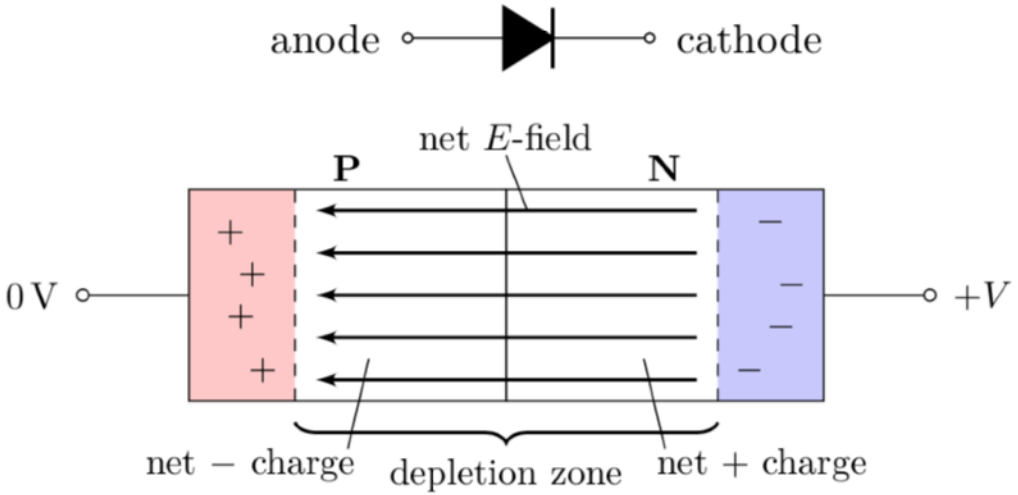


Changing V_{GS} will vary the depletion region and change the current.

This is a junction FET (jFET) where a p-type region is implanted within an n-type bulk. The depletion region can be controlled by the gate. Lower V_G increases the depletion.

$$I = n A q v$$

So changing the gate voltage controls nA and I. Like pinching off a hose. "Depletion mode"



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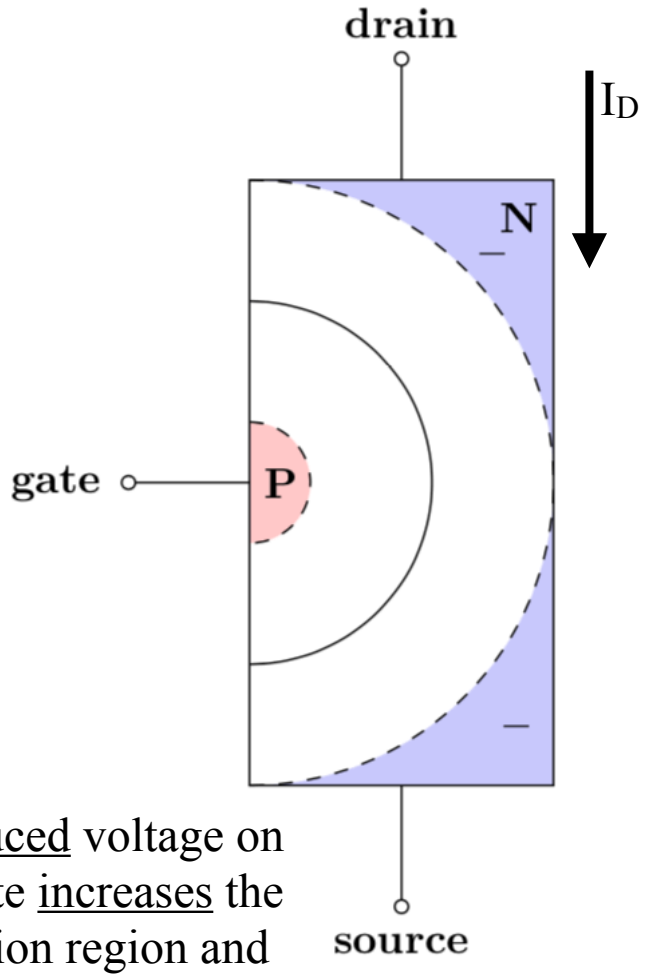

A reduced voltage on the gate increases the depletion region and reduces the current.

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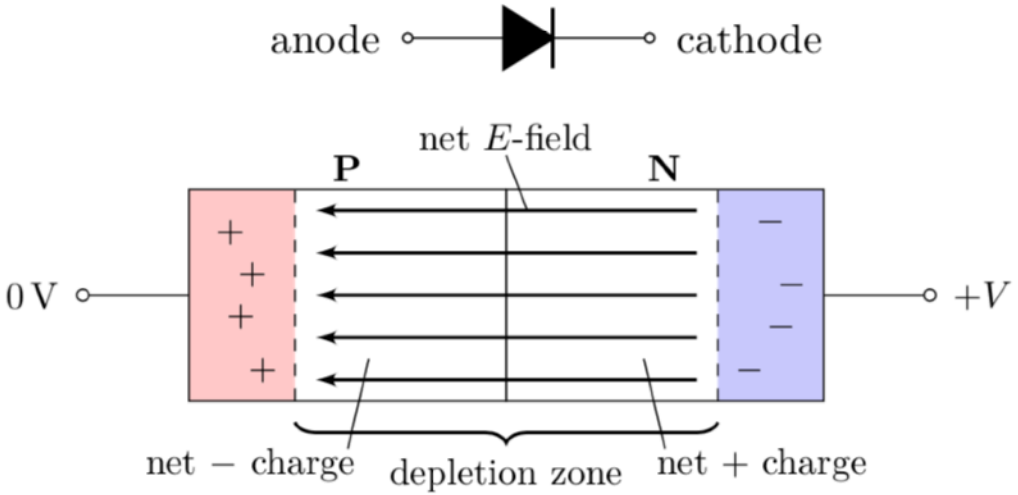

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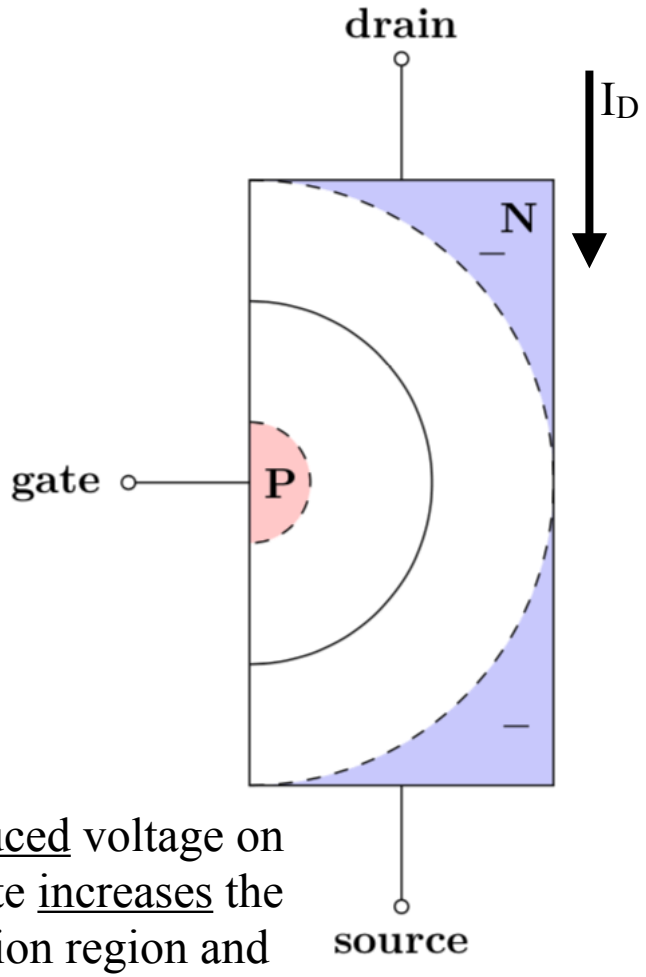

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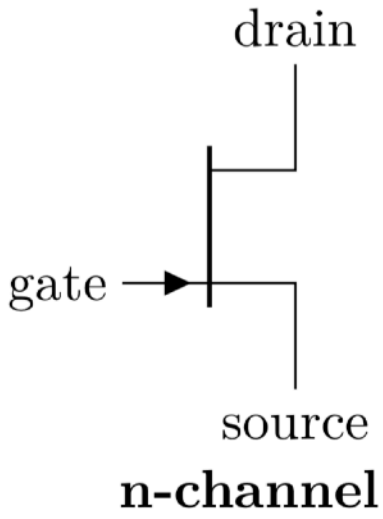

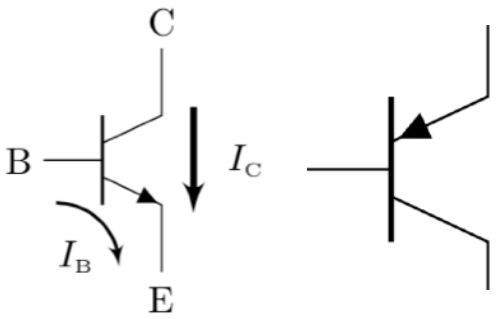

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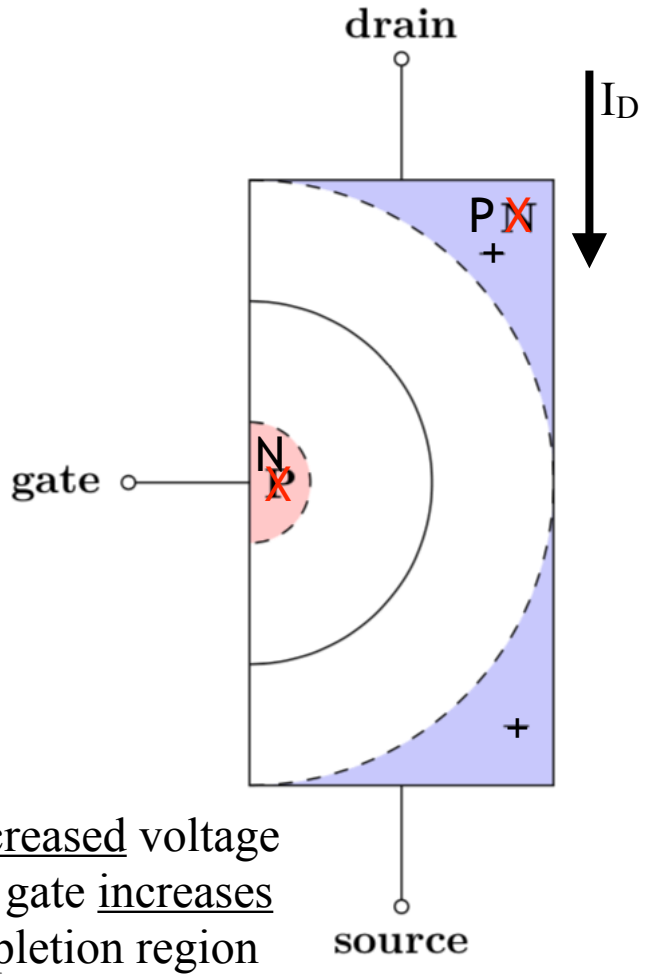
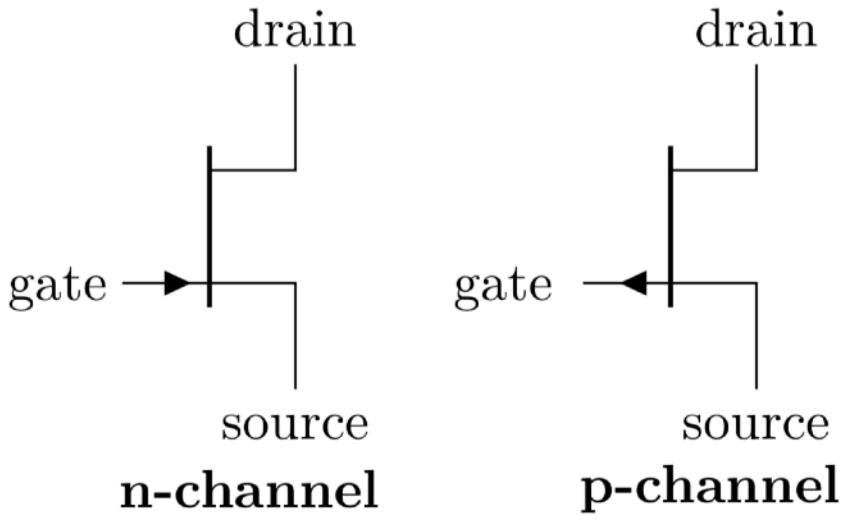


An increased voltage on the gate increases the depletion region and reduces the current.

This is a junction FET (jFET) where a p-type region is implanted within an n-type bulk. The depletion region can be controlled by the gate. Lower V_G increases the depletion.

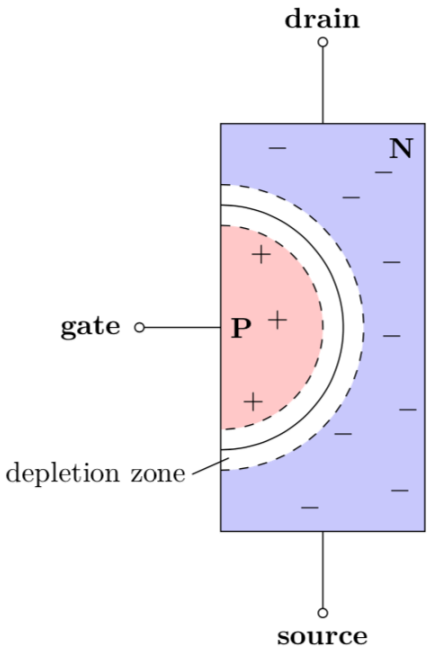
$$I = n A q v$$

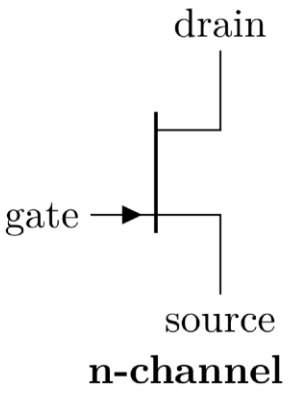
So changing the gate voltage controls nA and I. Like pinching off a hose. "Depletion mode"



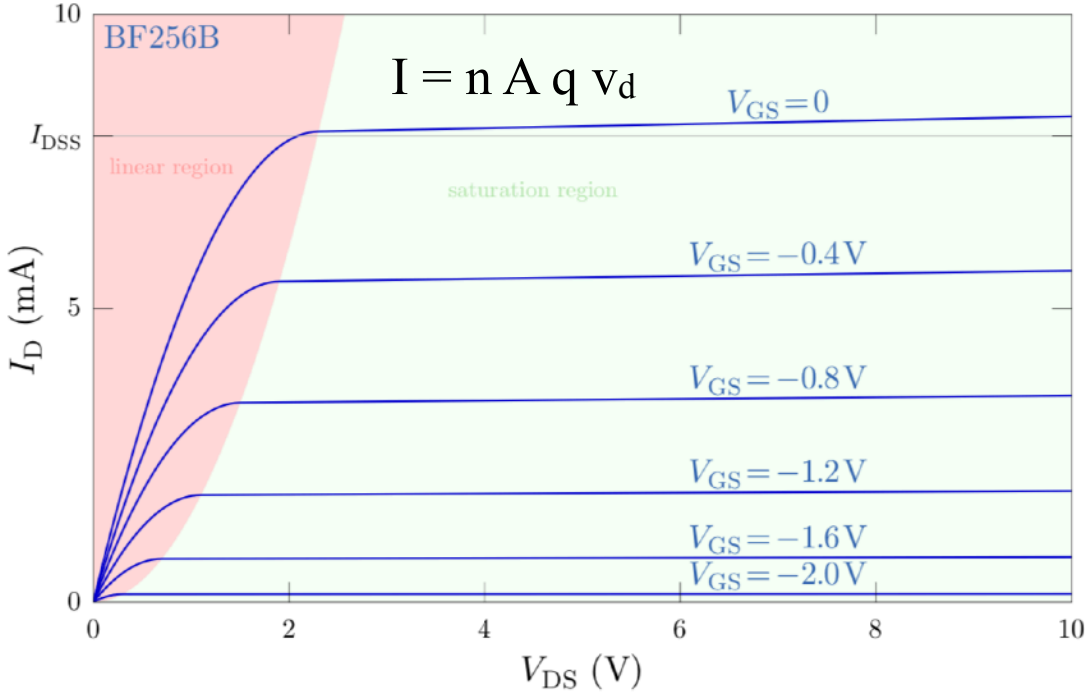
Field effect transistors (JFETs)

The current is controlled by V_{GS}.





If $V_{GS} = 0$ current flows, saturating at I_{DSS} based on doping.
If $V_{GS} > 0$ a bit more current flows.



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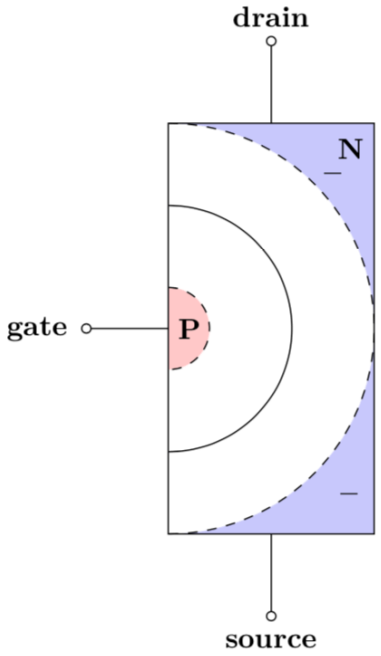
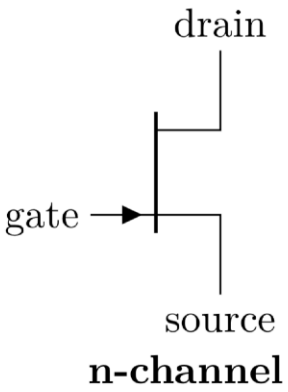
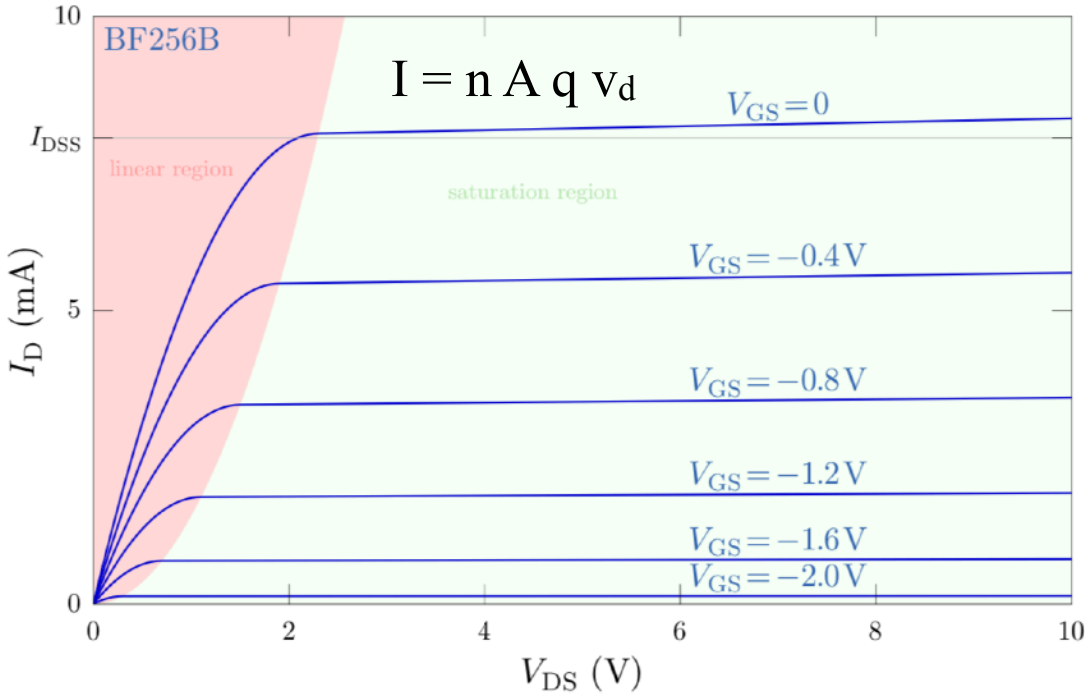


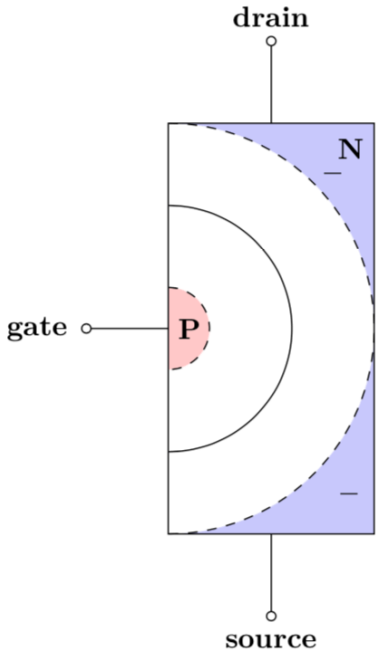


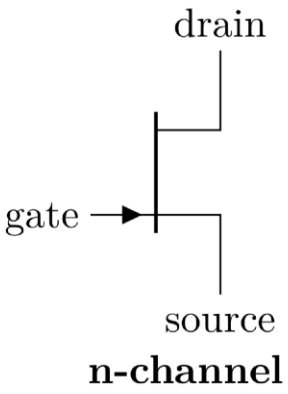
If $V_{GS} = 0$ current flows, saturating at I_{DSS} based on doping.
If $V_{GS} > 0$ a bit more current flows.
If $V_{GS} < 0$ less current flows.
If $V_{GS} < V_\Theta$ then $I_D = 0$. V_Θ is typically a couple volts.
So a voltage (E field) controls a current, like the Ebers-Moll view, but depleting the current.



Field effect transistors (JFETs)

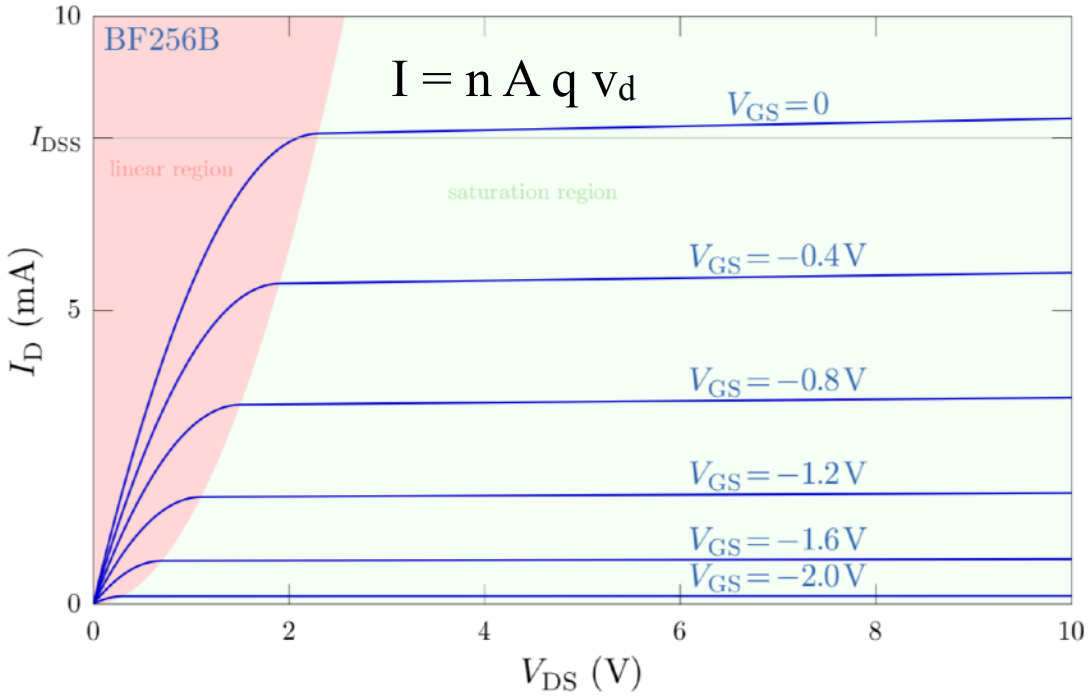
In the linear region, it behaves like a voltage-controlled resistor:





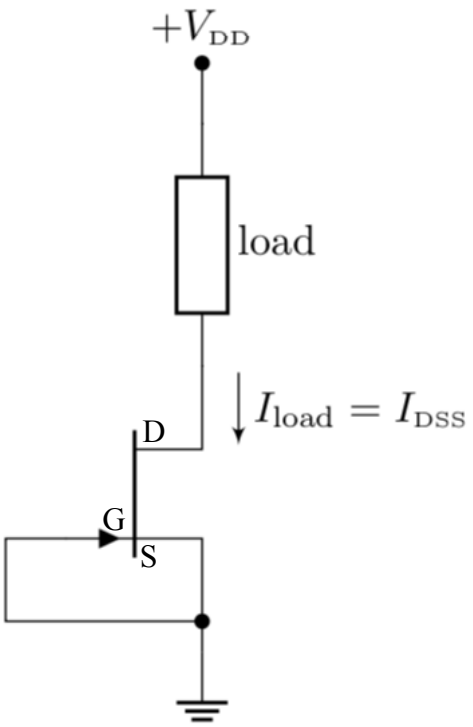
$$I_D = 2k\left[(V_{GS} - V_\Theta)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$R \cong \frac{1}{2k(V_{GS} - V_\Theta)}.$$

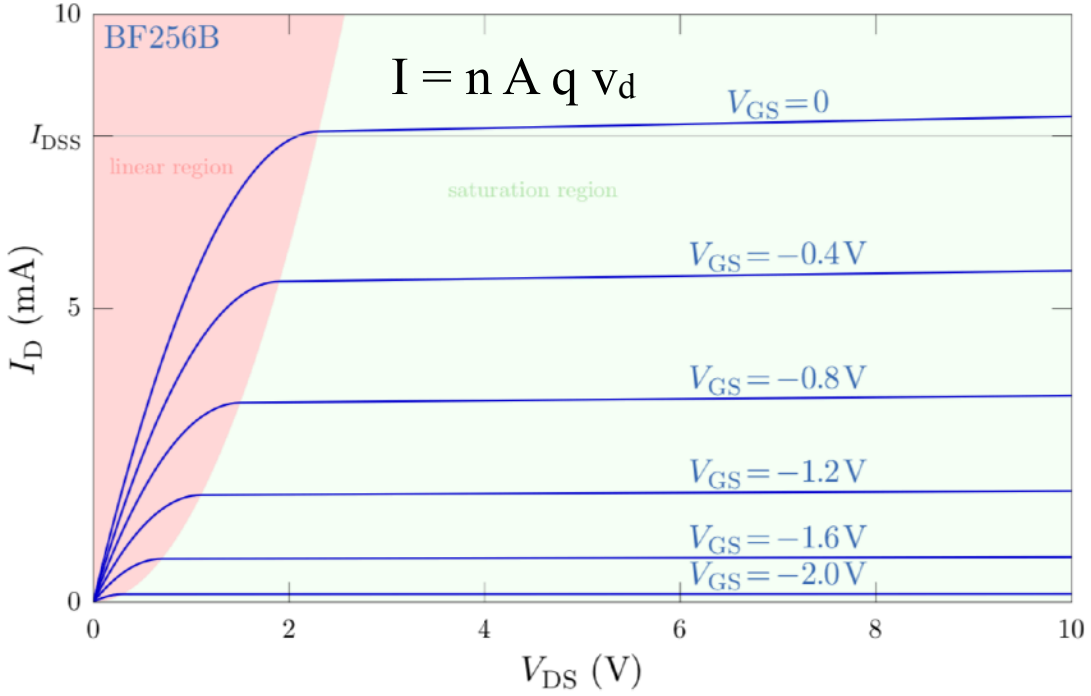


Field effect transistors (JFETs)

In saturation region, behaves like a voltage-controlled current source:



$$I_D = k(V_{GS} - V_\Theta)^2$$



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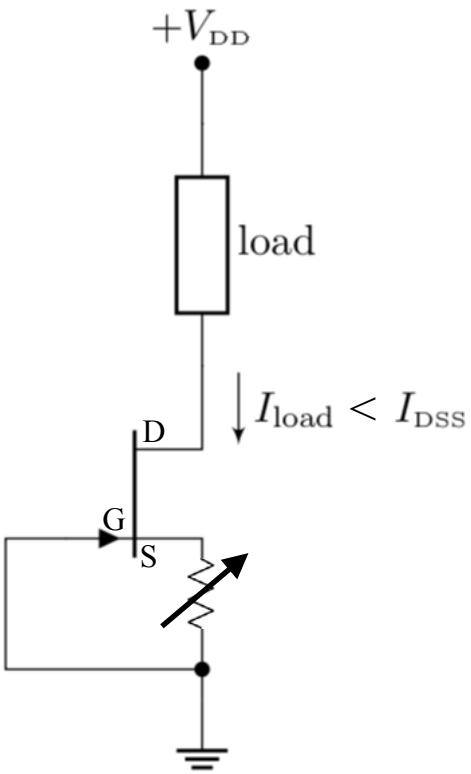

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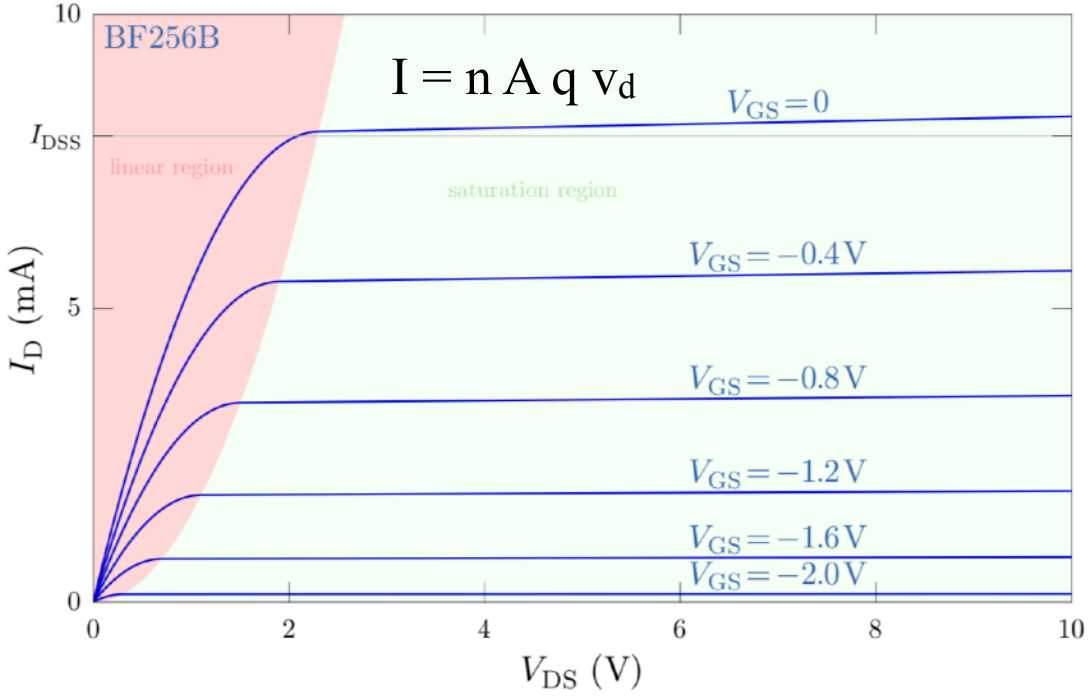

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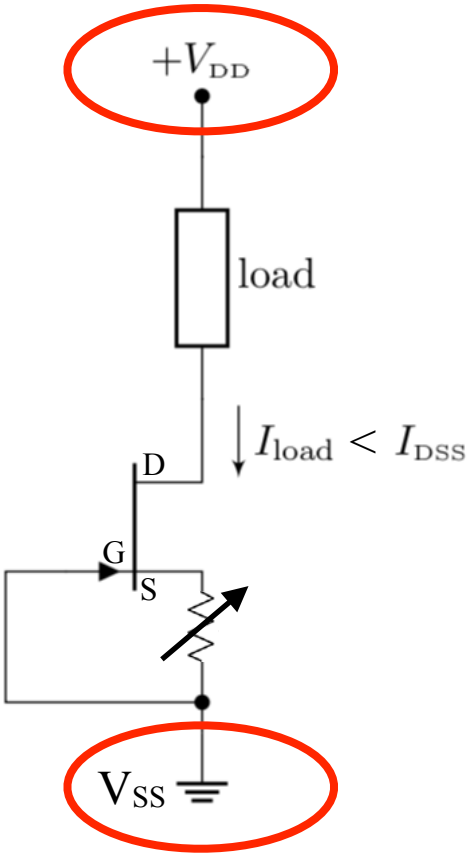
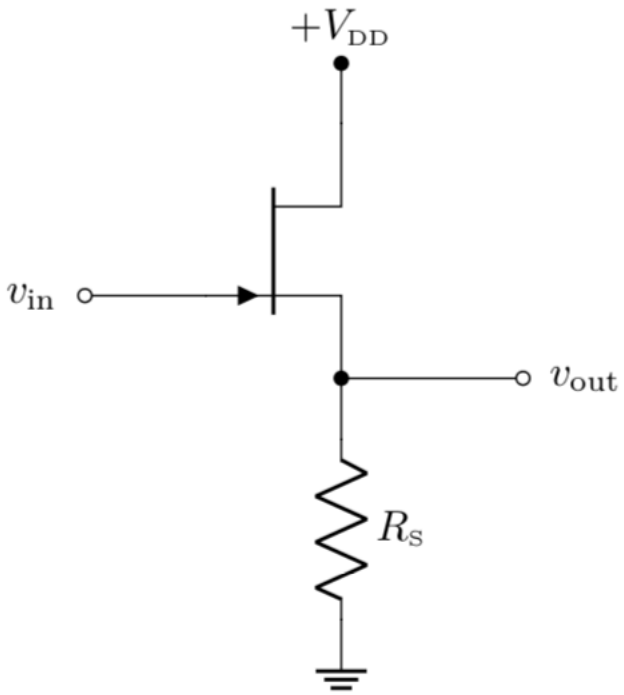


Now the power supplies are called V_{DD} and V_{SS} instead of V_{CC} and V_{EE}

Field effect transistors (JFETs)

Can build the same transistor circuits: source follower



Change in V_{GS} changes current flow, so there is a transconductance relation:

$$i_D = g_m v_{GS}$$

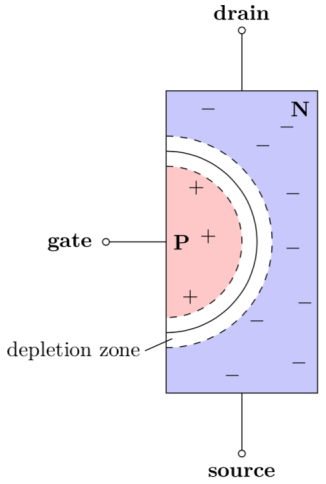
This is from taking delta's of the linear region current relation

$$I_D = 2k\left[(V_{GS} - V_\Theta)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

So,

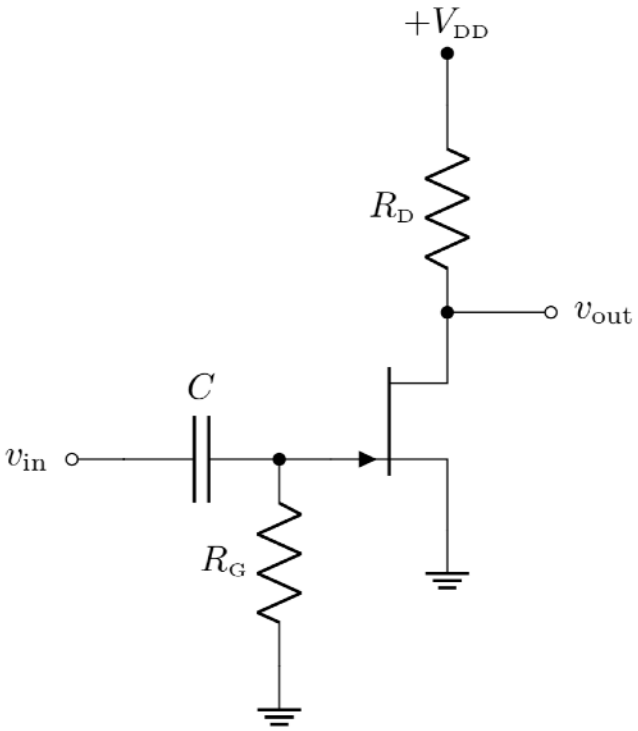
$$v_S = i_{DS} R_S$$

and that is V_{out}.



Field effect transistors (JFETs)

Can build the same transistor circuits: common-source amplifier



Again we have

$$i_D = g_m v_{GS}$$

And the output voltage varies as

$$v_{out} = v_D = -i_D R_D$$

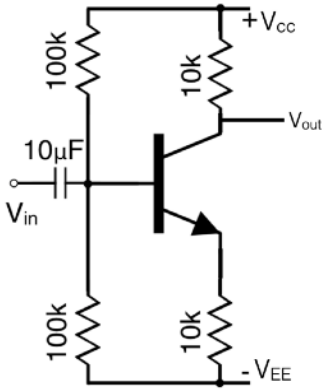
$$v_{out} = -g_m R_D v_{in}$$

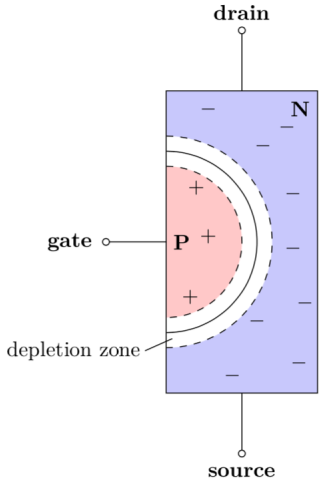
So,

$$G = -g_m R_D$$

The transconductance, g_m, is mho and about 1/200Ω. So large R_D gives large negative gain.

Note: no biasing above ground required, just R_G to hold DC at ground.





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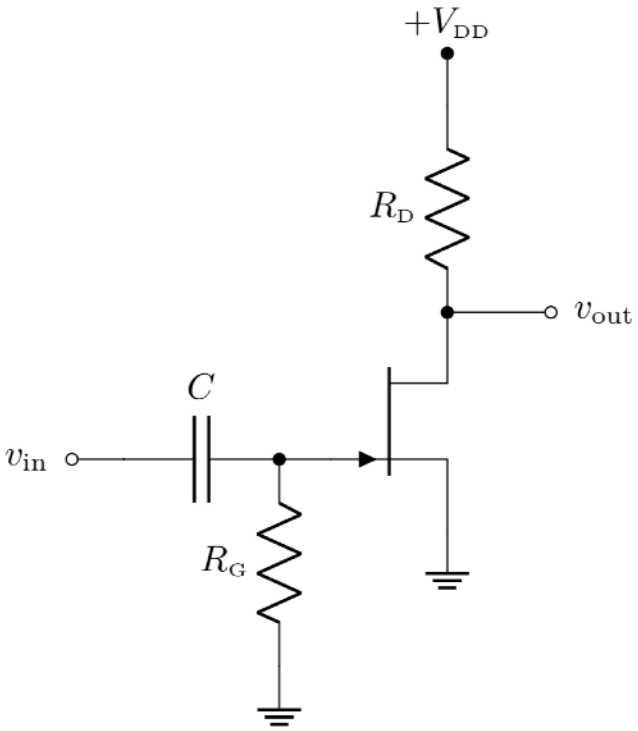

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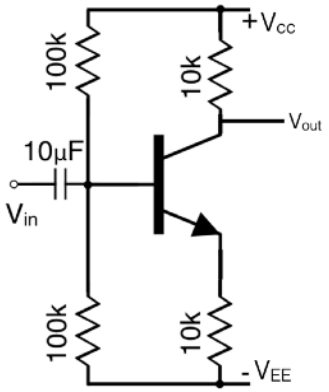
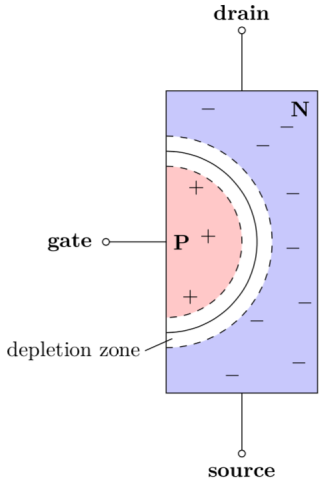
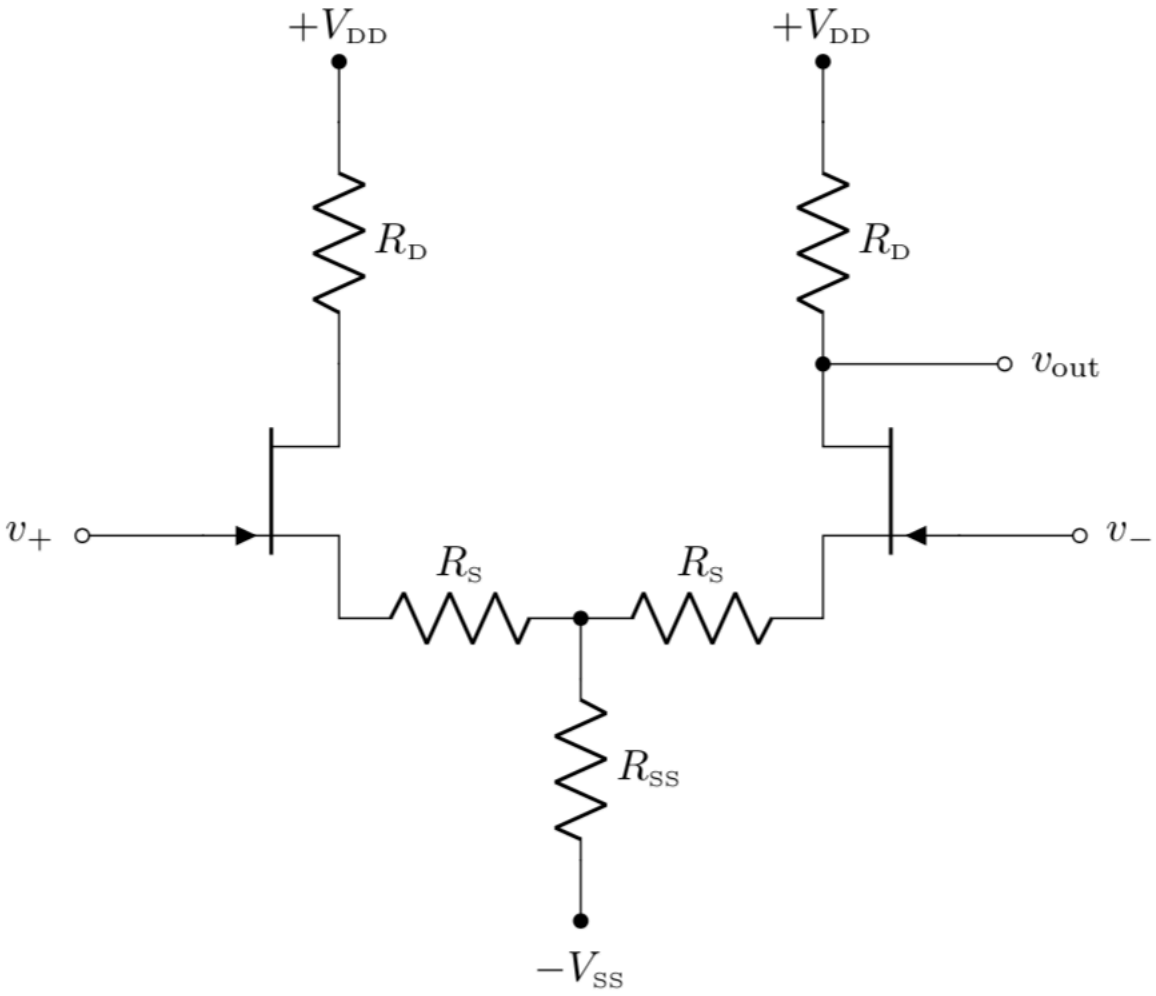




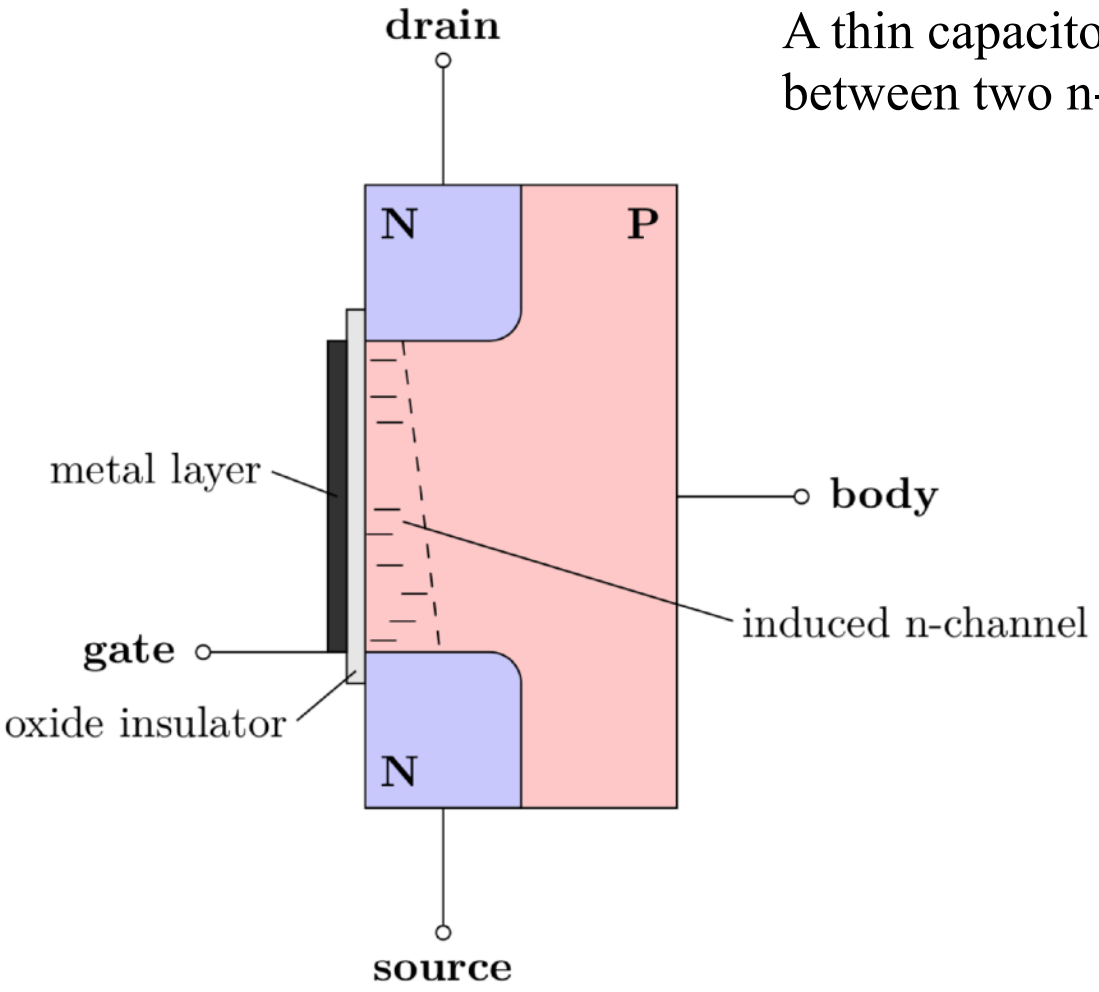
Field effect transistors (JFETs)

Can build the same transistor circuits: differential amplifier



Field effect transistors (MOSFETs)

Another type of FET uses a metal-oxide-semiconductor based capacitor rather than a junction to control the gate. MOSFET



A thin capacitor is placed over a p-type region between two n-types.

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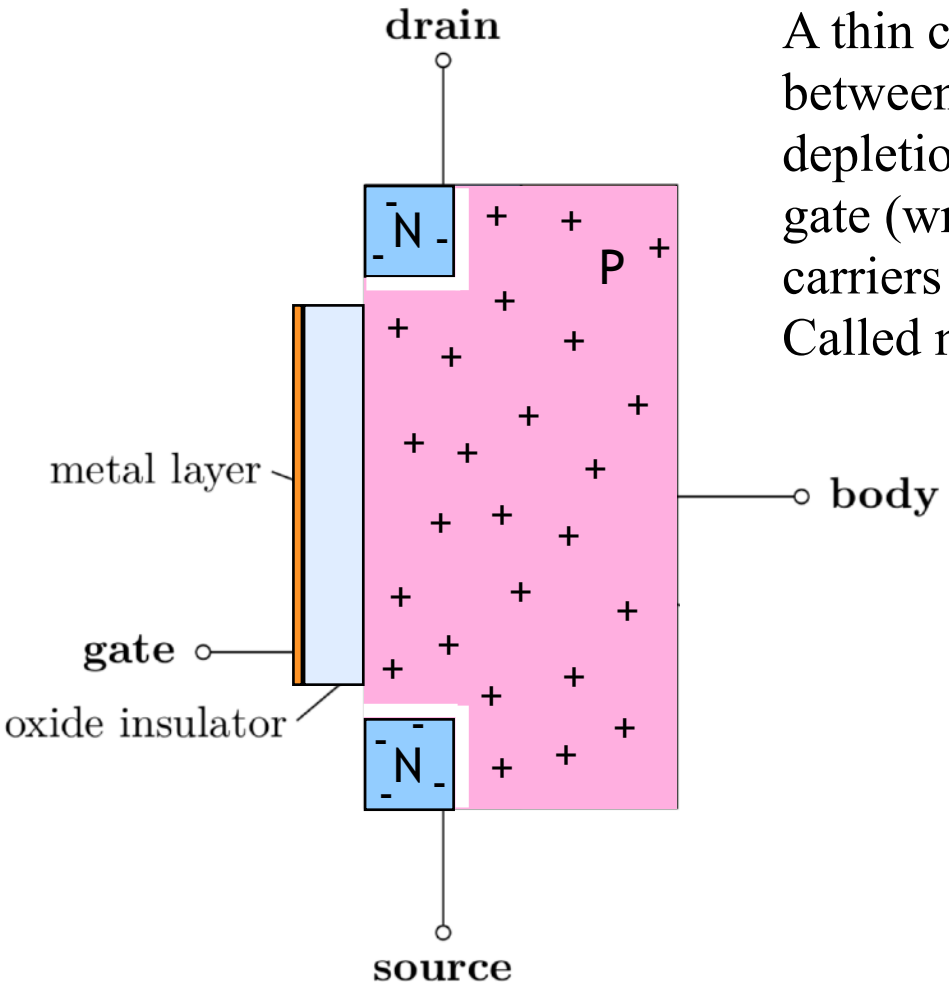

A thin capacitor is placed over a p-type region between two n-types. No current flows because of depletion regions. But a positive voltage on the gate (wrt the body) induces negative charge carriers in the p-type region.
Called n-channel since n-type carriers move.

Field effect transistors (MOSFETs)

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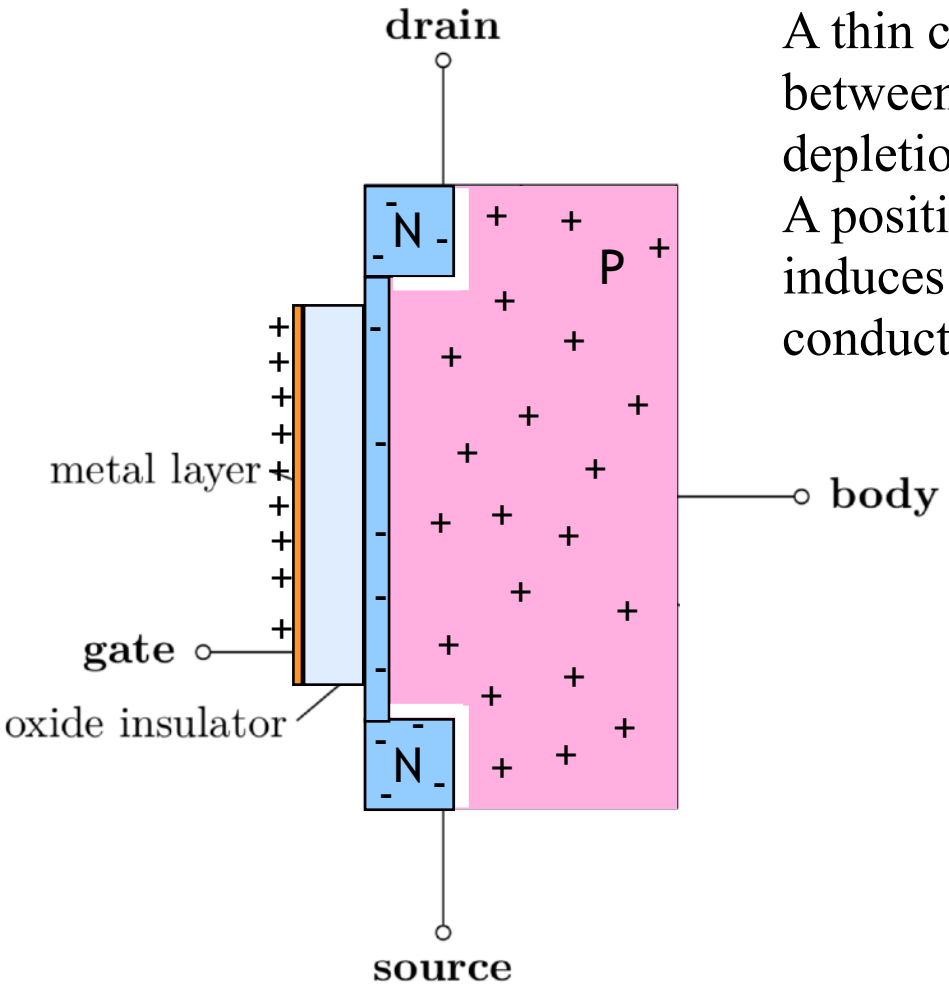
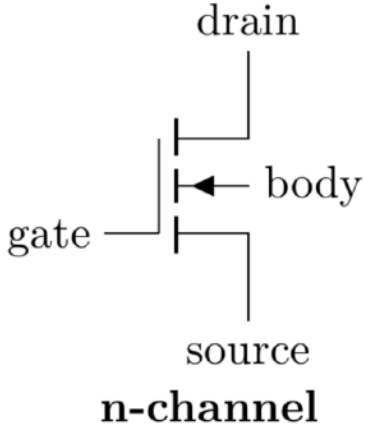


A thin capacitor is placed over a p-type region between two n-types. No current flows because of depletion regions.

A positive voltage on the gate (wrt the body) induces negative charge carriers to form a conduction channel — an n-channel.

This is an "enhancement mode" FET, where no current flows until a voltage (relative to the body) allows it.



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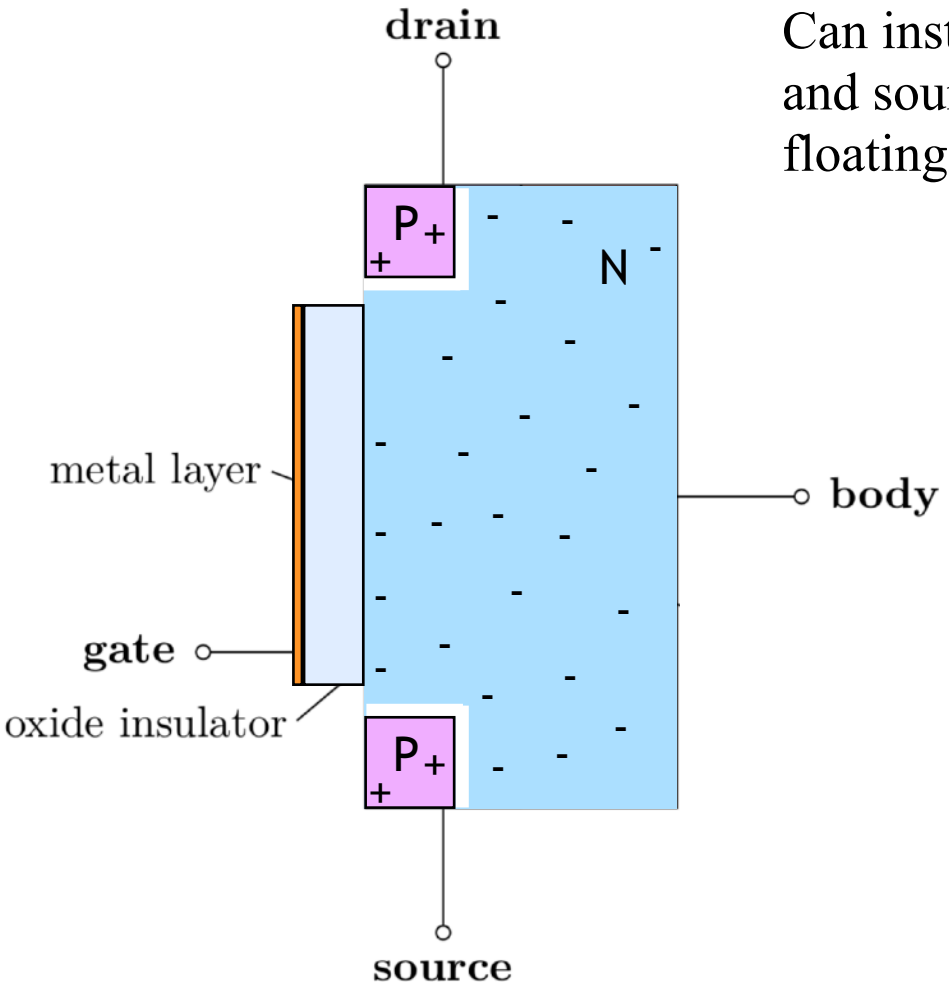

Can instead use an n-type bulk with p-type drain and source implants. Again, no current if gate floating.

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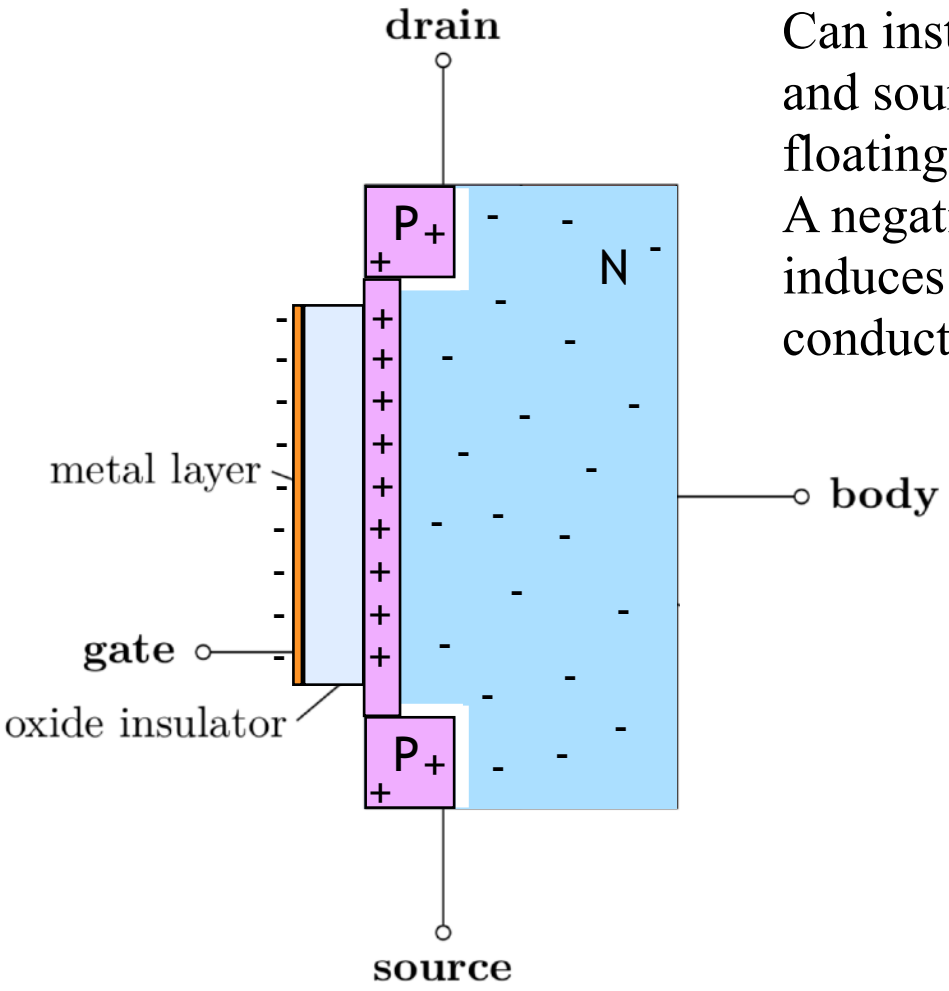
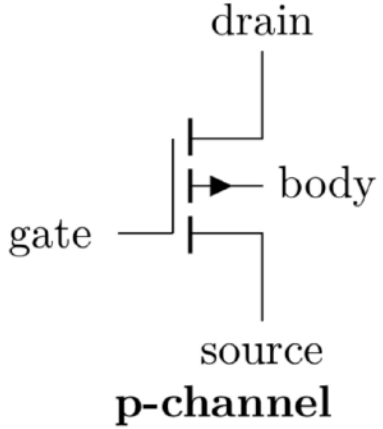


Can instead use an n-type bulk with p-type drain and source implants. Again, no current if gate floating.

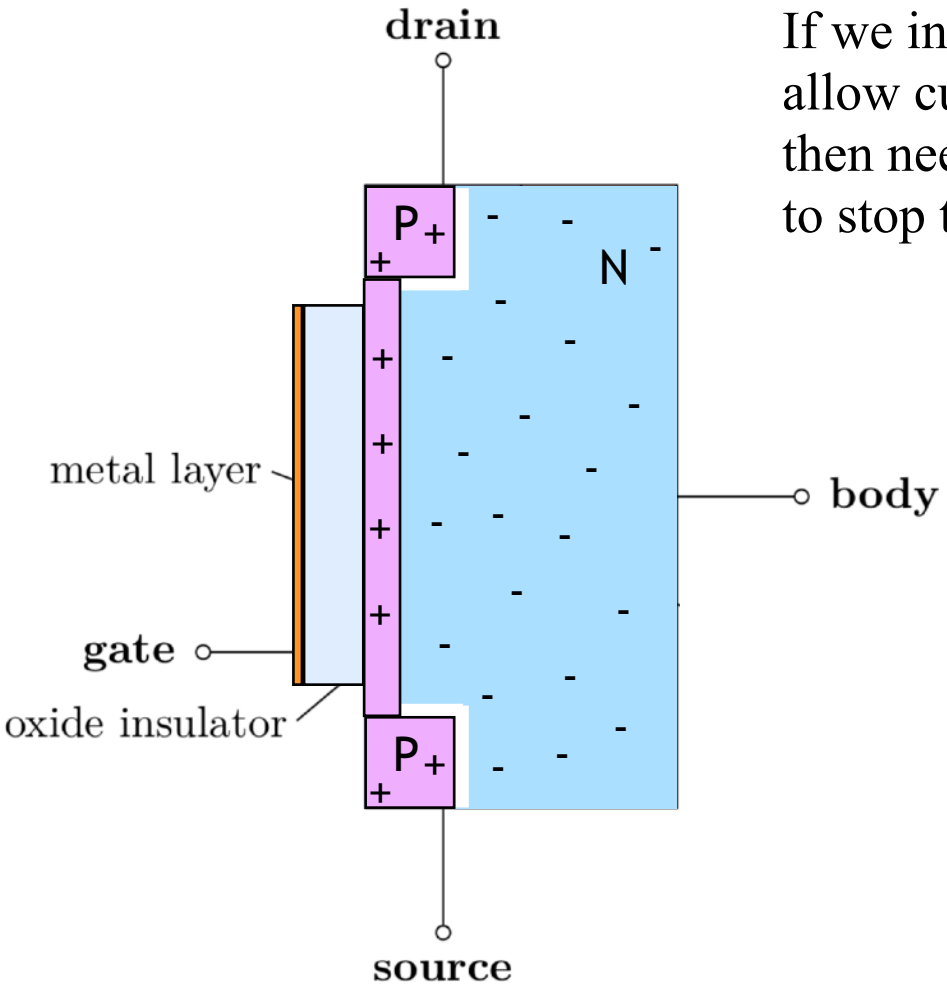
A negative voltage on the gate (wrt the body) induces positive charge carriers to form a conduction channel — a p-channel.



"Enhancement mode" since current normally off.

Field effect transistors (MOSFETs)

We can also make depletion mode MOSFETs



If we introduce a channel of charge carriers that allow current to flow with the gate floating, we then need to push them away with a gate voltage to stop the current.

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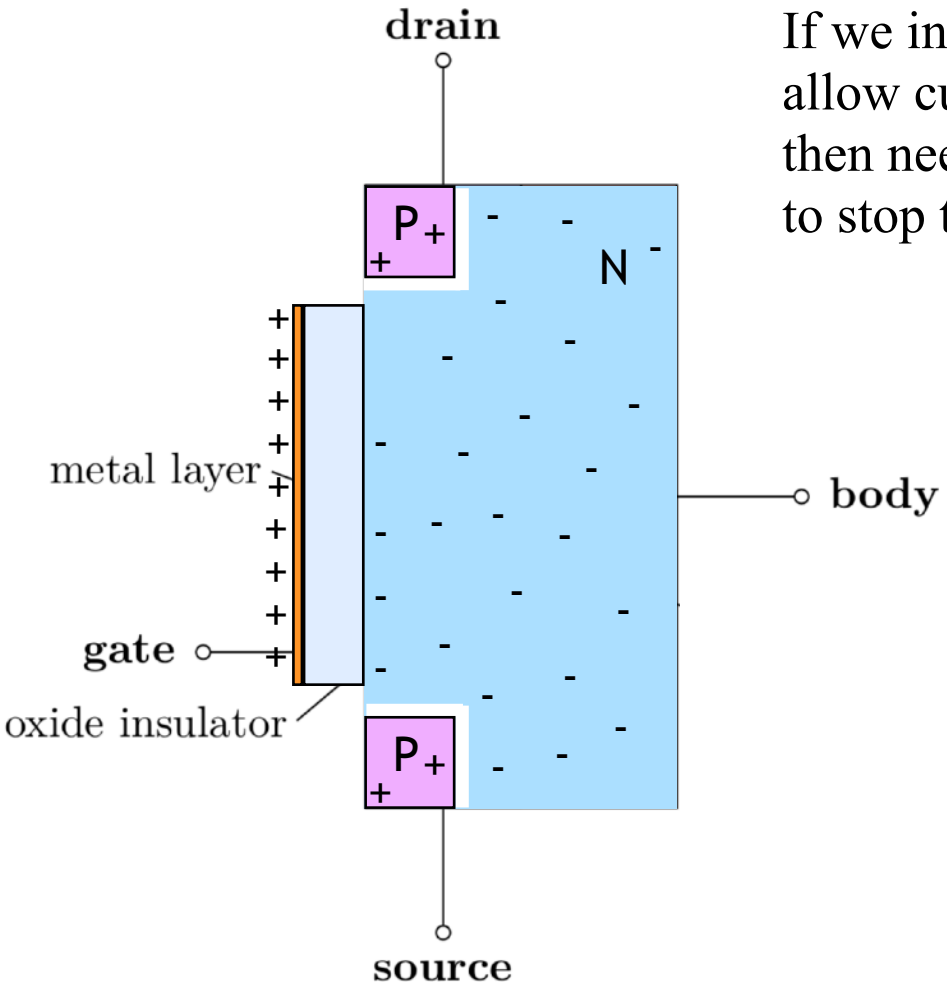

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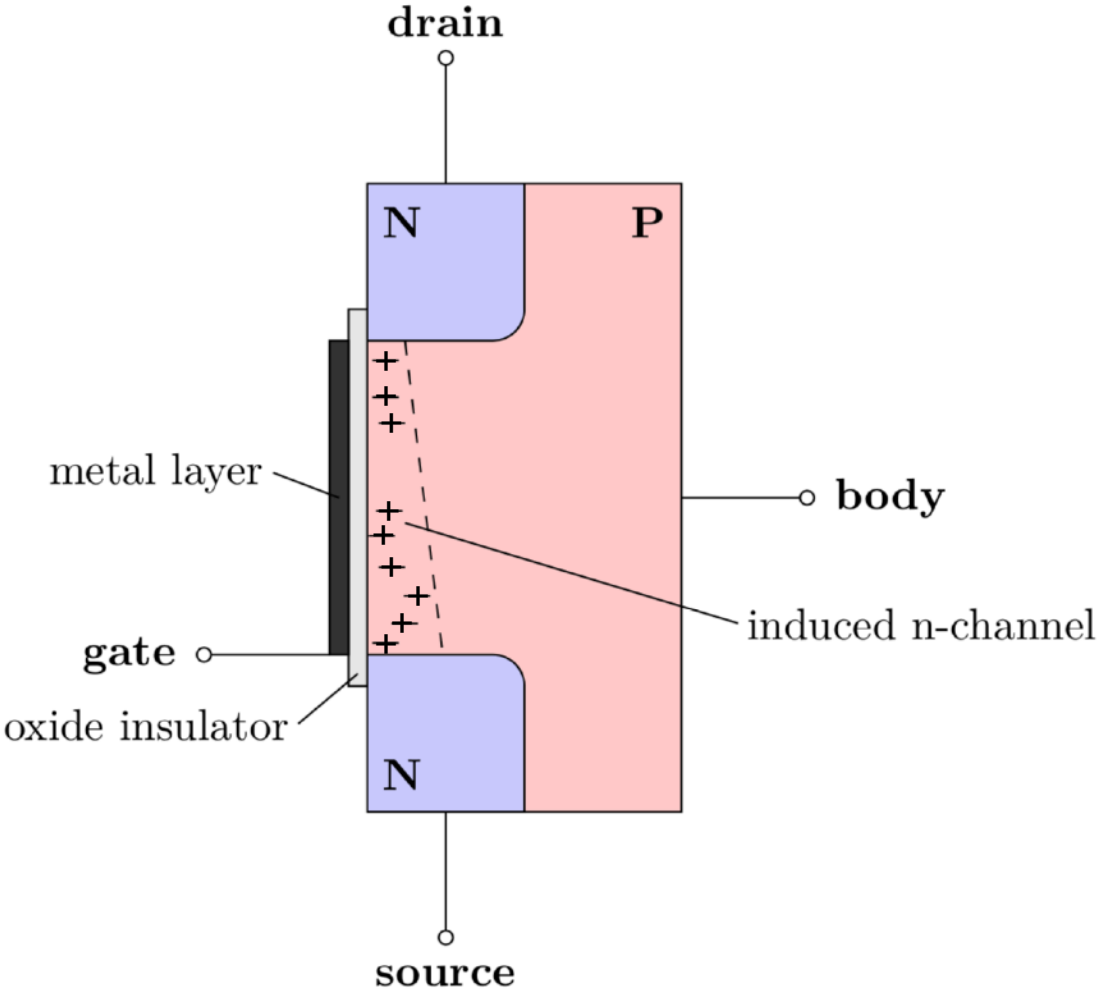
Field effect transistors (FETs)

Electro-static discharge (ESD) is a risk for MOSFETs due to thin oxide.



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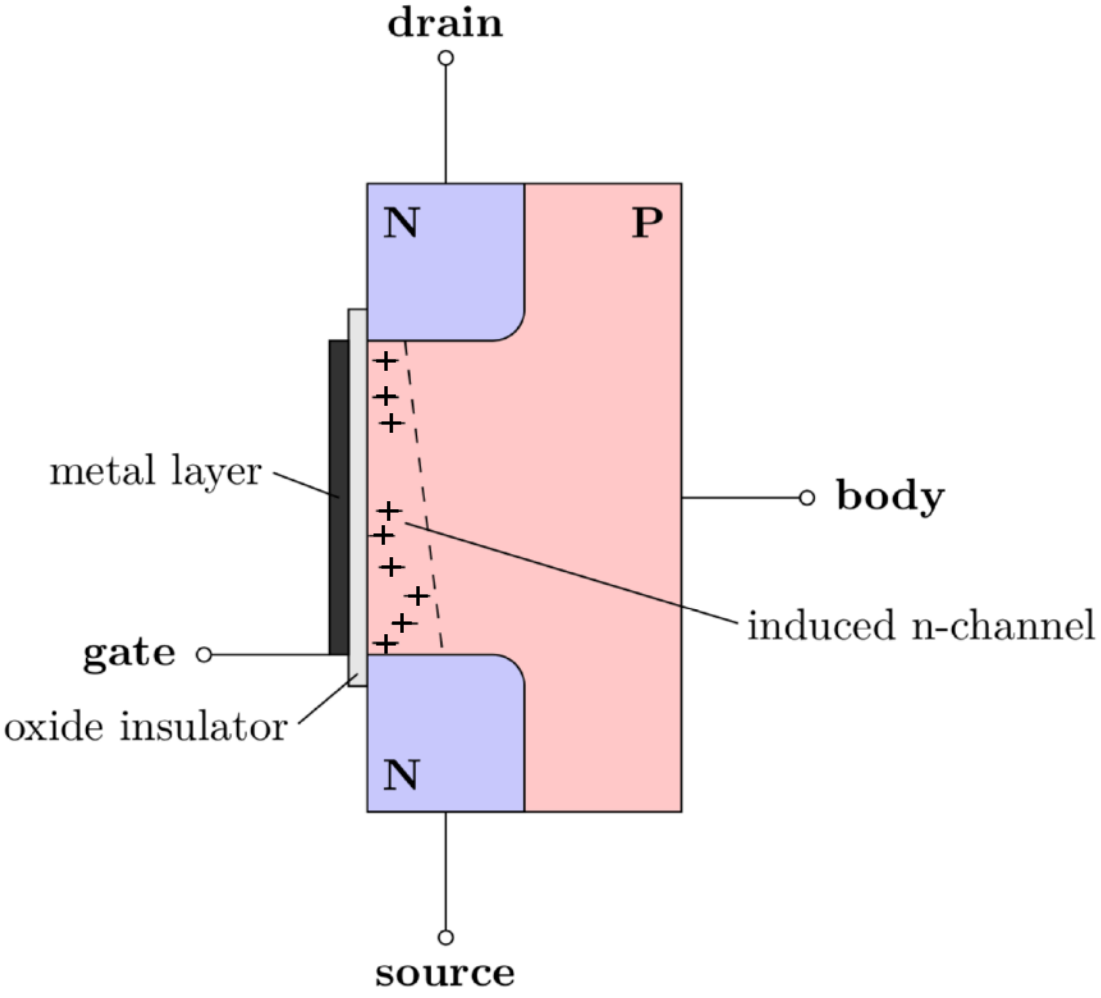

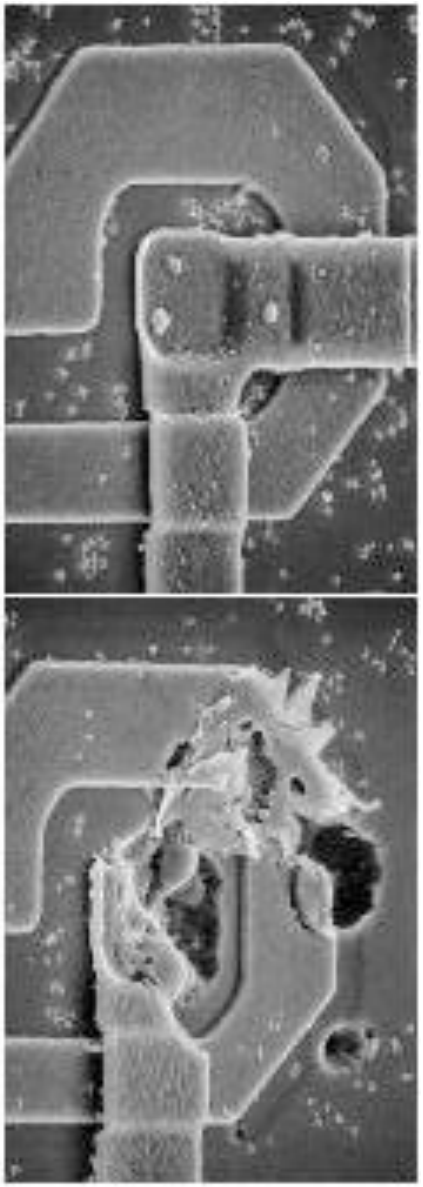

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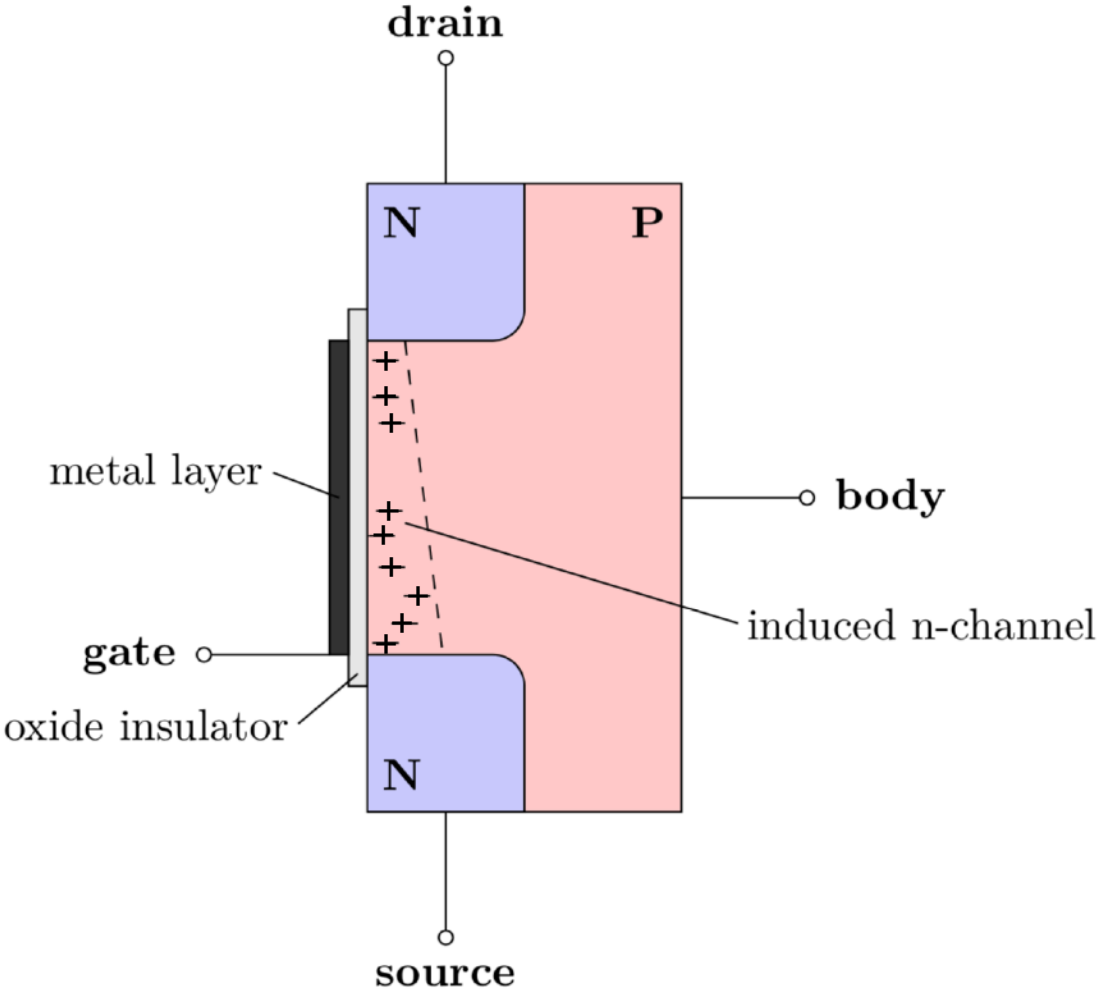
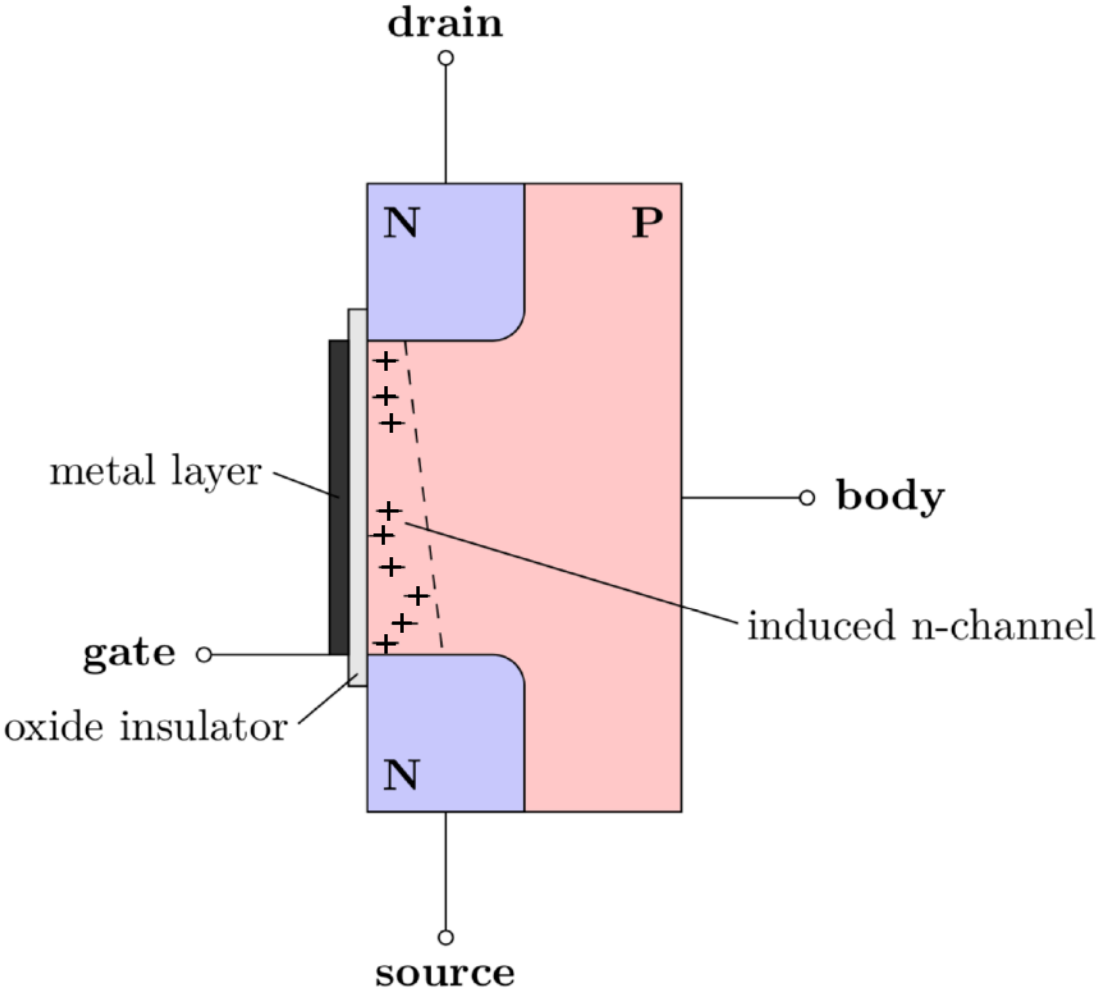


Field effect transistors (FETs)

Note that the MOSFET has large input impedance since little current flows through capacitor; just induces charge to enable I_D current flow.



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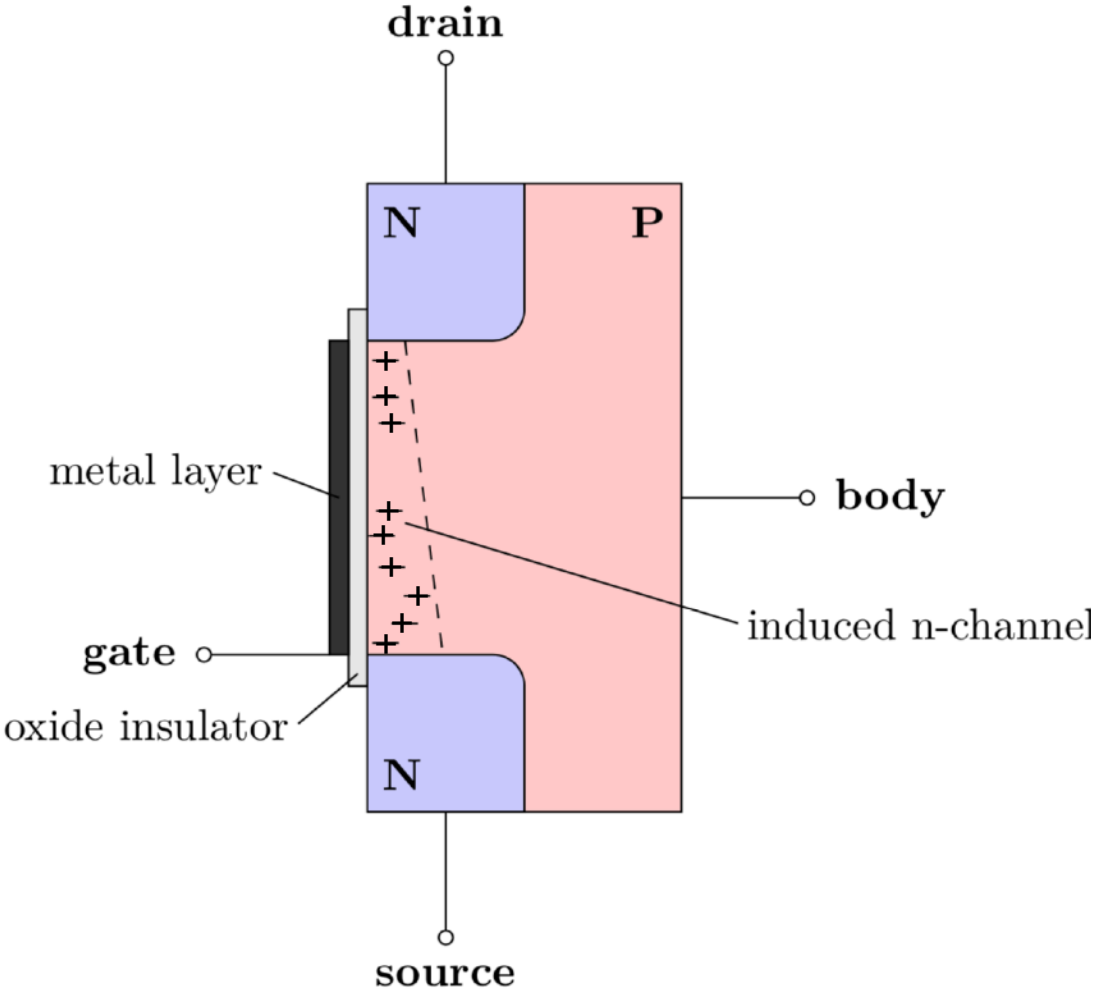
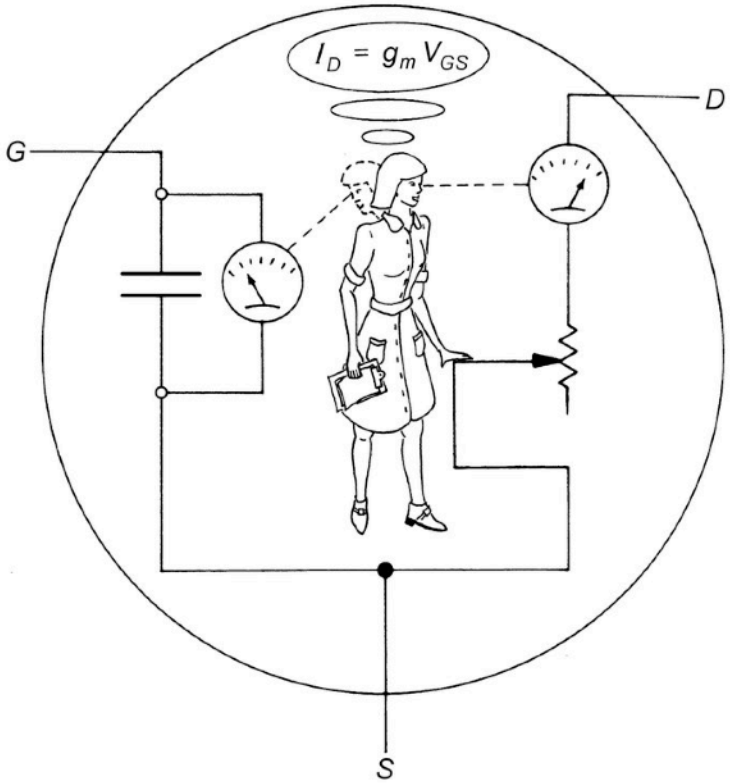
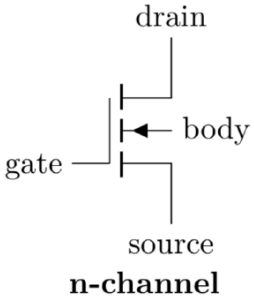


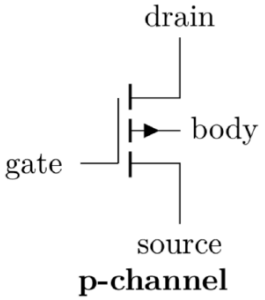


MOSFET switches

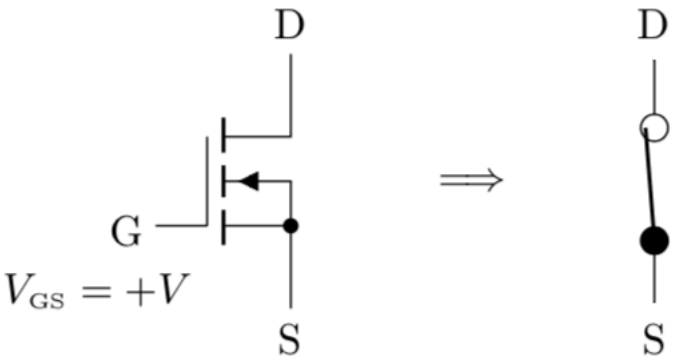
MOSFETs are useful as switches

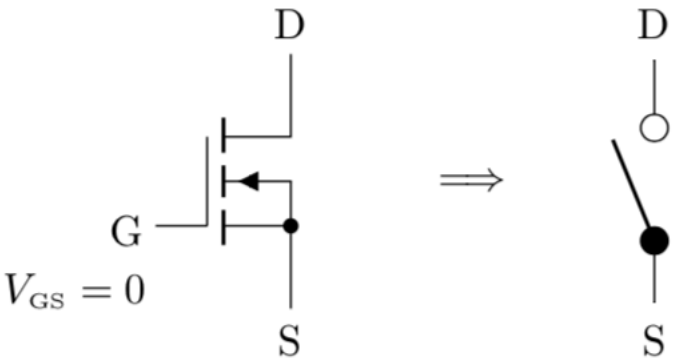


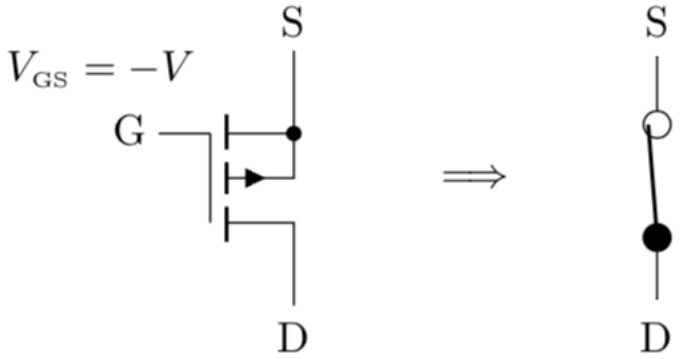
On with gate high

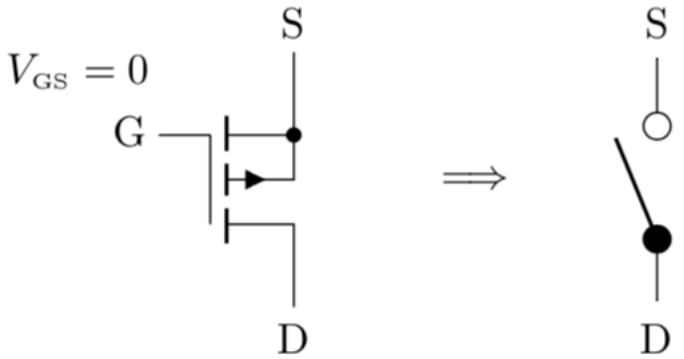


On with gate low









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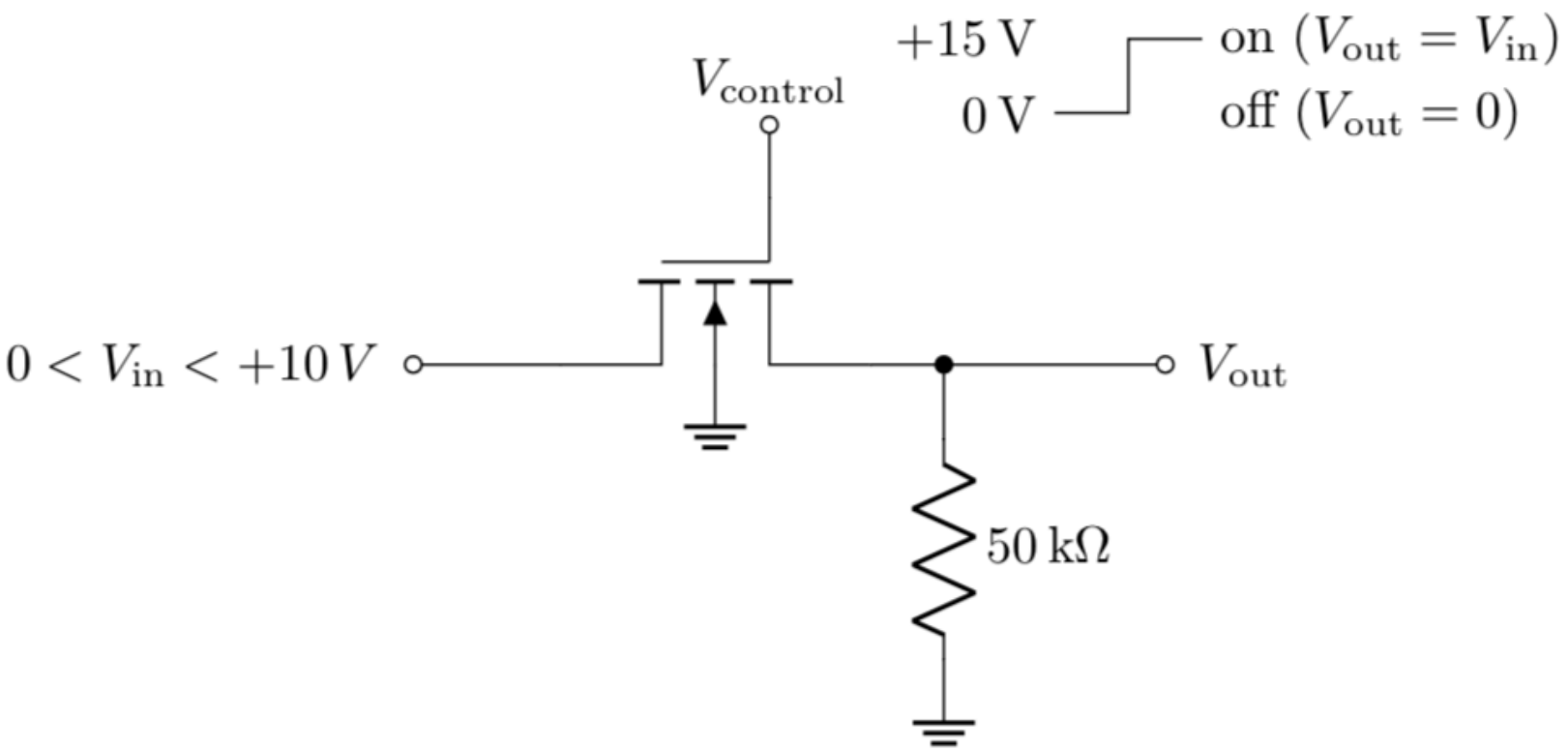
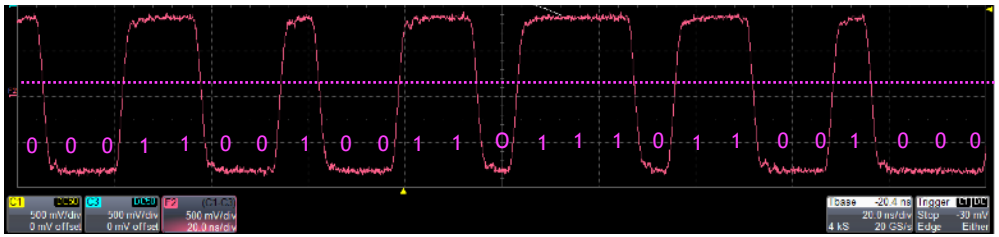
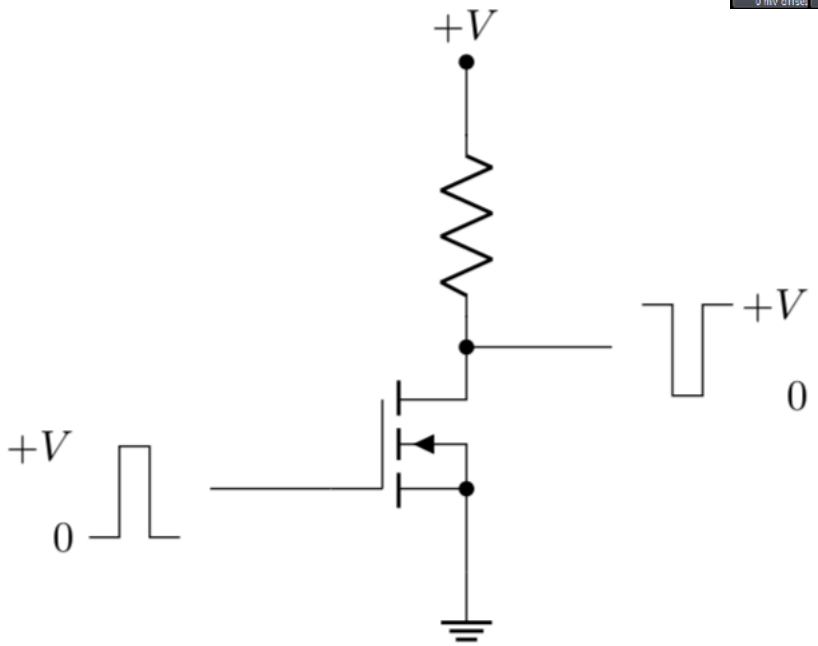


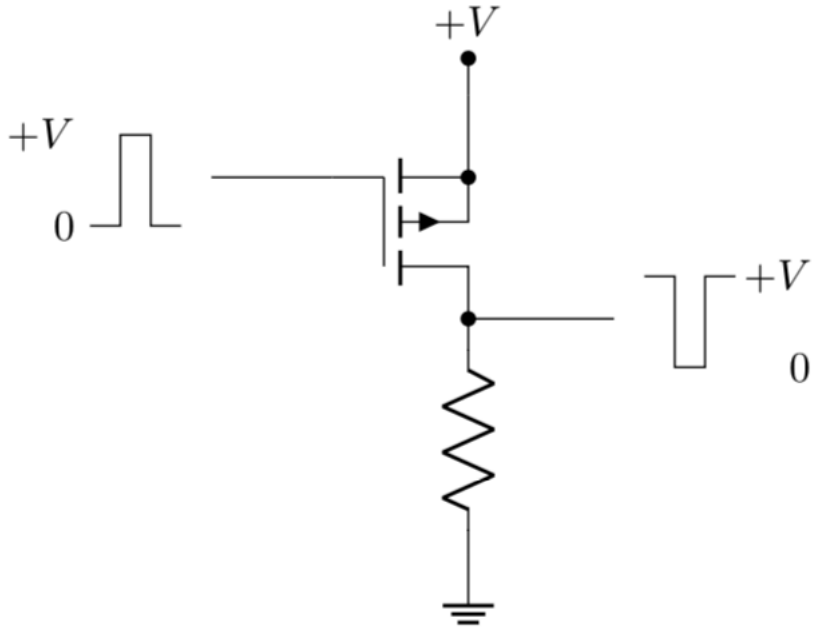
MOSFETs are useful for logic

For inputs and outputs that are at V_{DD} or V_{SS} only, we can represent logic high and logic low signals and perform logic operations.

MOSFET inverter







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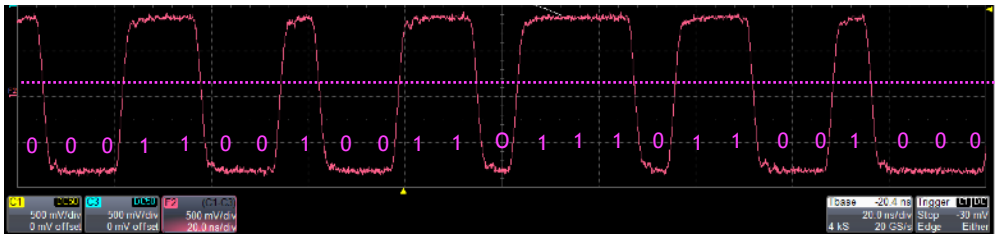
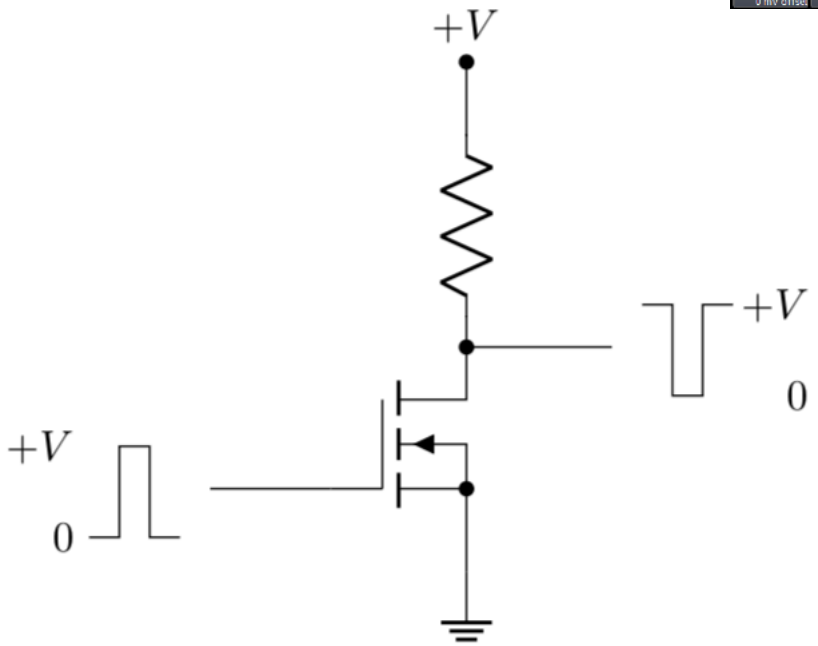
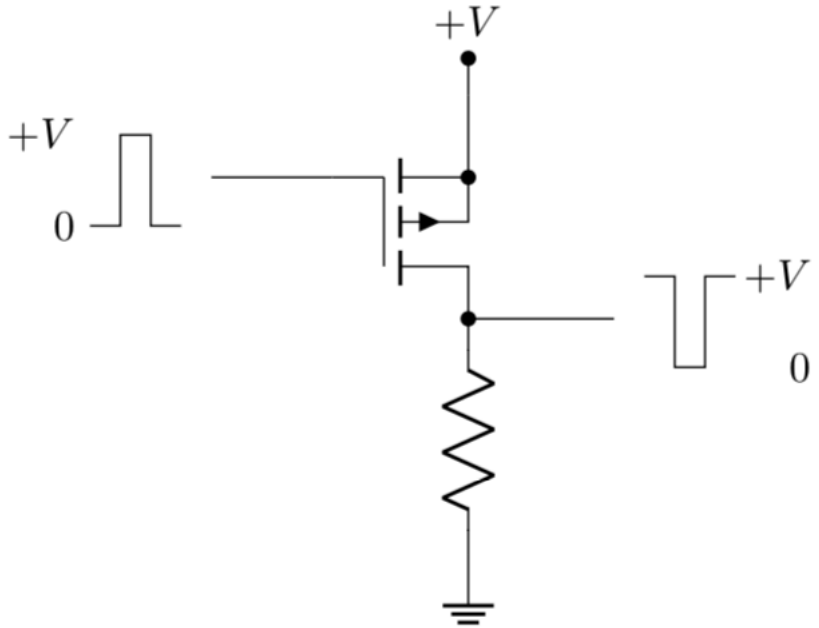


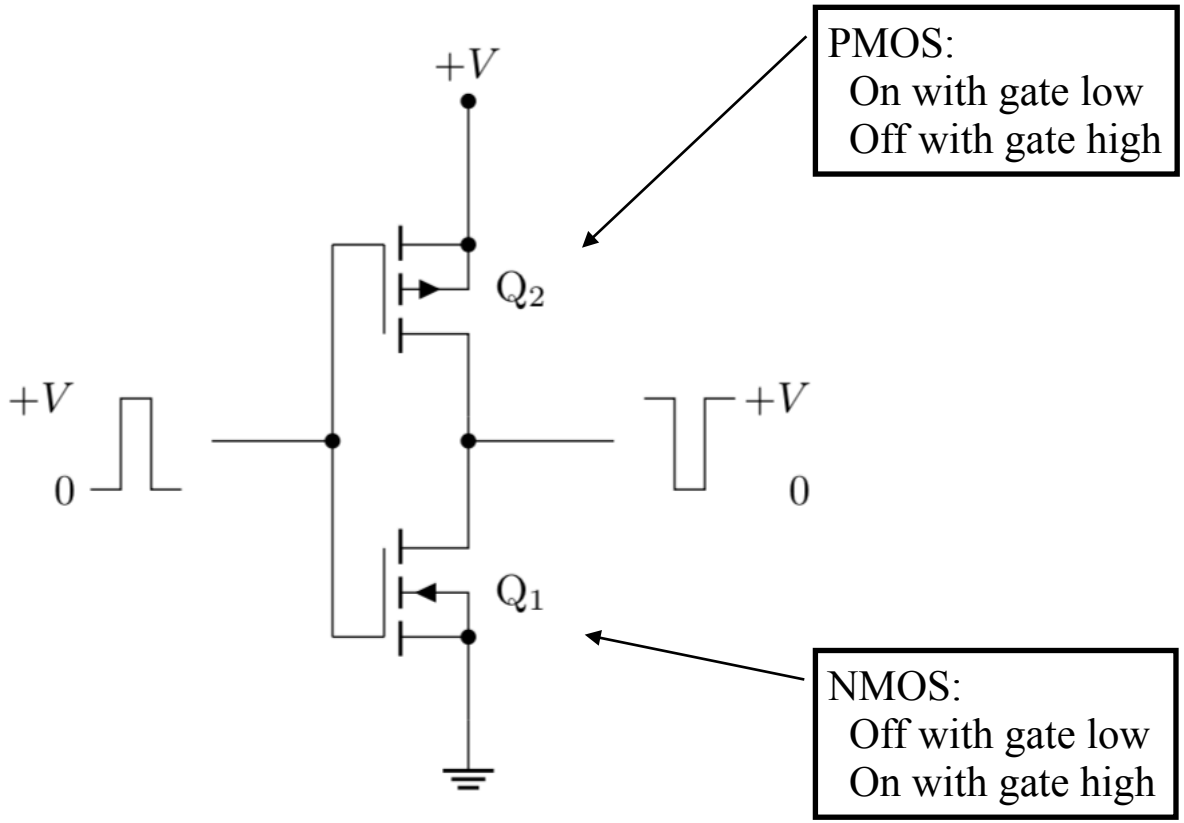




But resistors cost more than transistors in both space, €, and power…

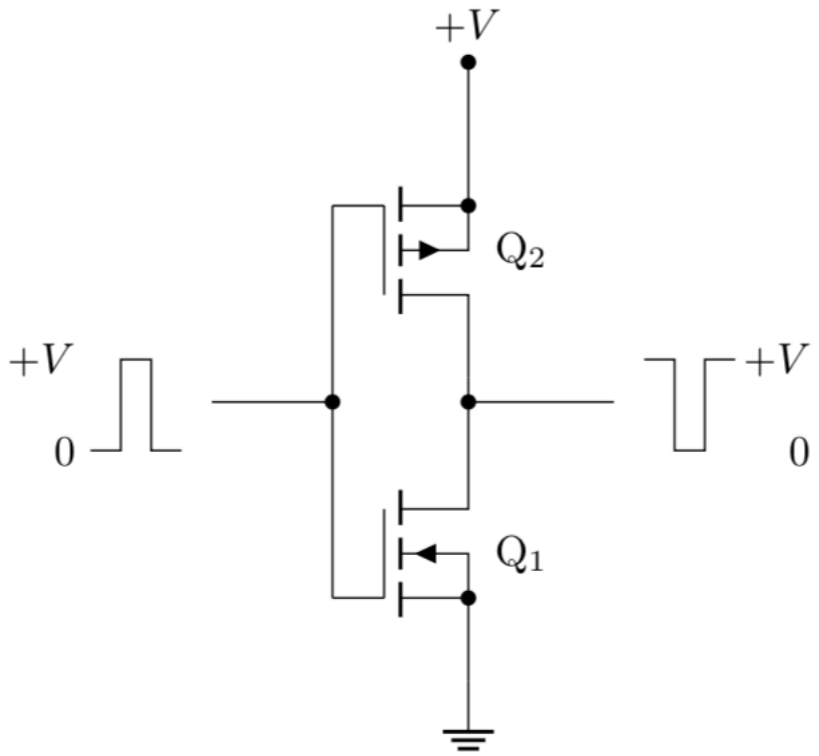
CMOS

Combining n-channel and p-channel MOSFETs together gives a balance of switching. Called, Complementary Metal-Oxide-Semiconductor Field Effect Transistors, or CMOS



CMOS

For inputs and outputs that are at V_{DD} or V_{SS} only, we can represent logic high and logic low signals and perform logic operations.
This is a logic NOT.



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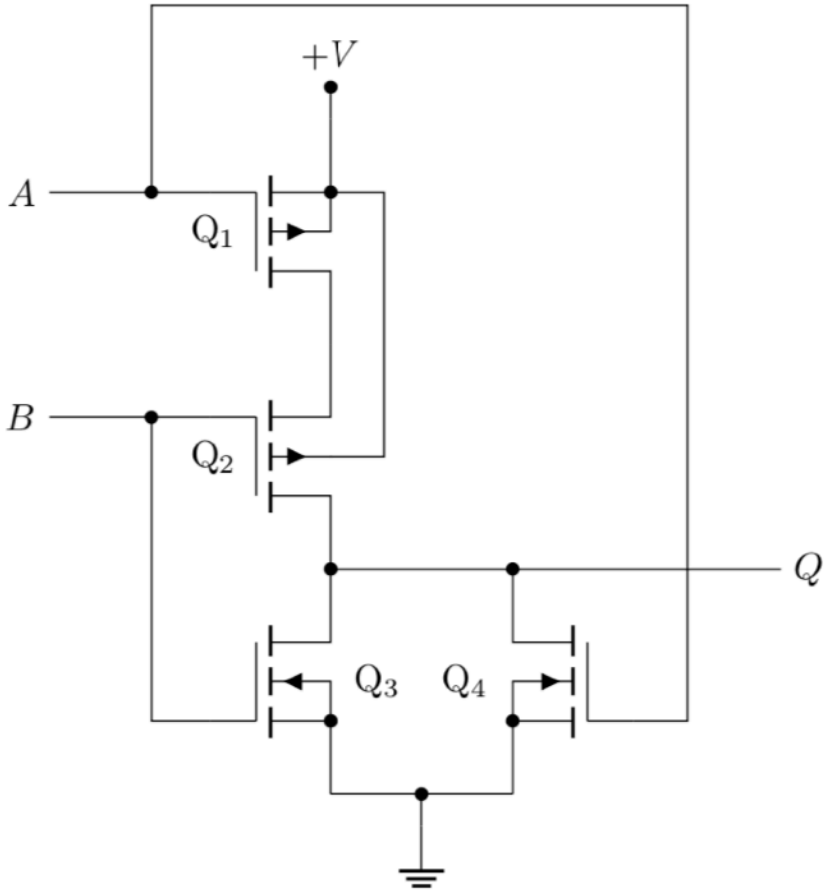

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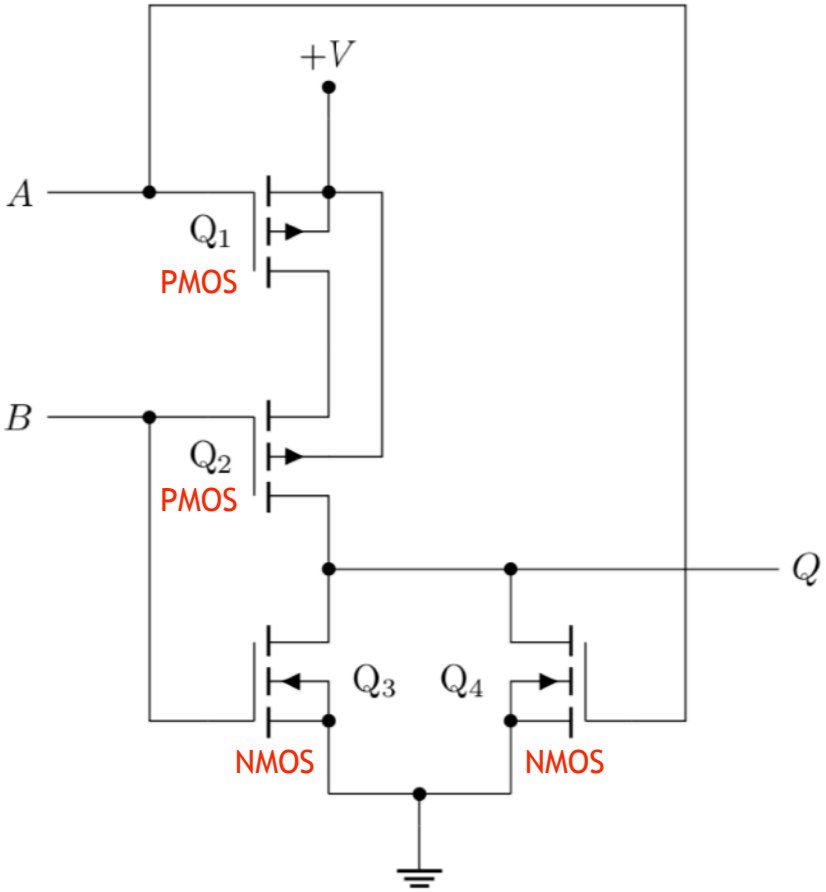

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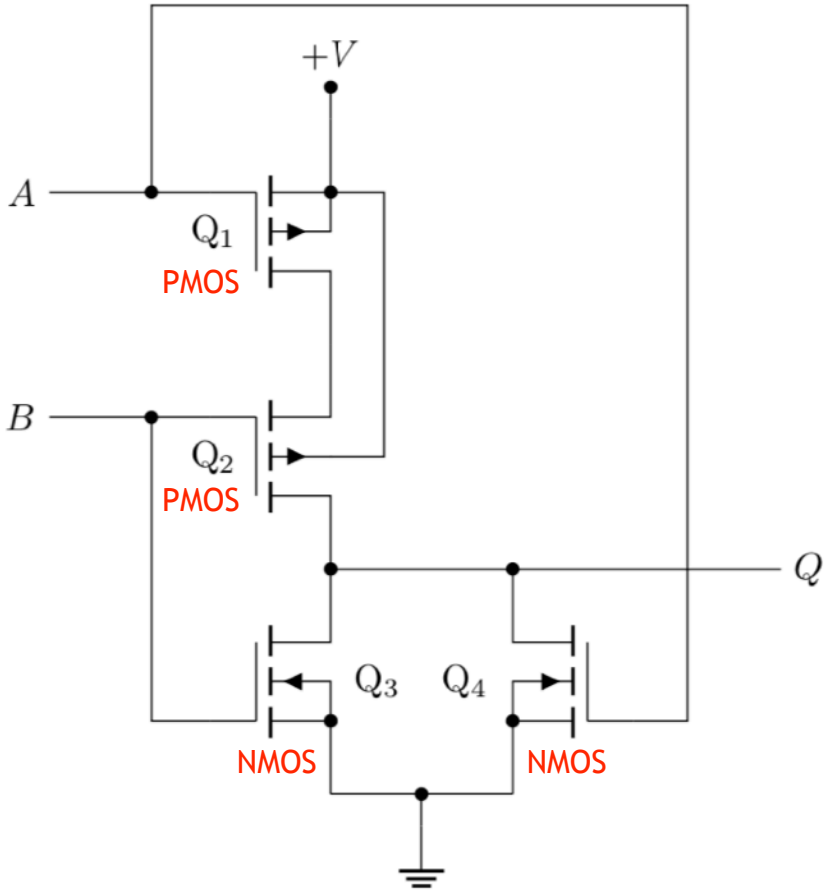

Truth table:

A	B	Q
0	0	
1	0	
0	1	
1	1	

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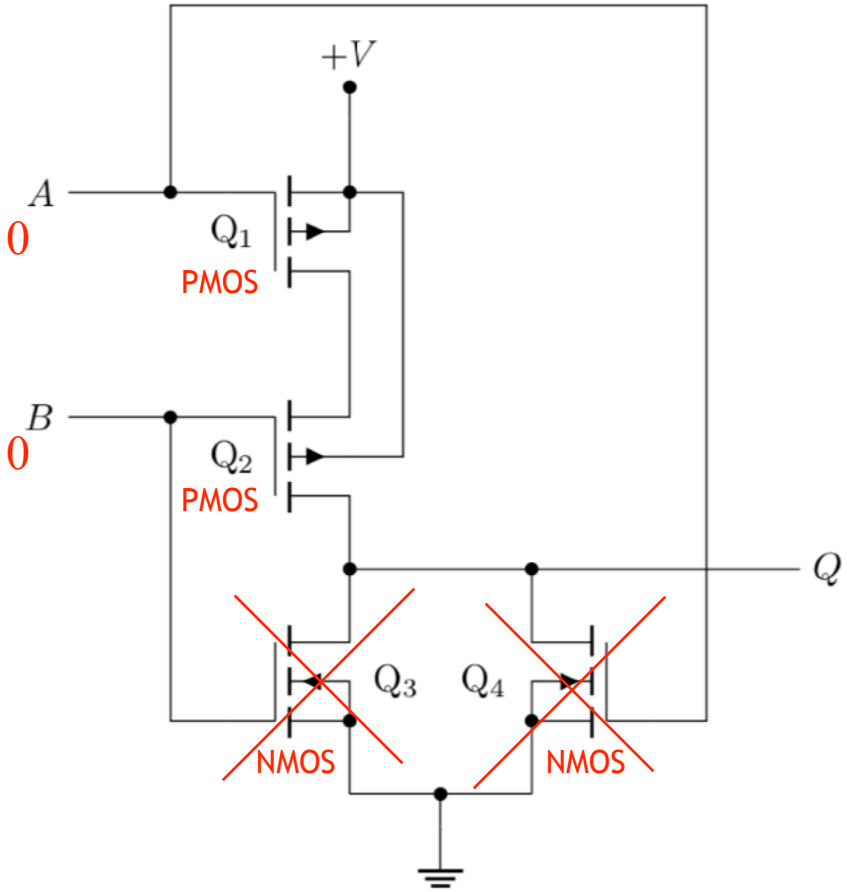

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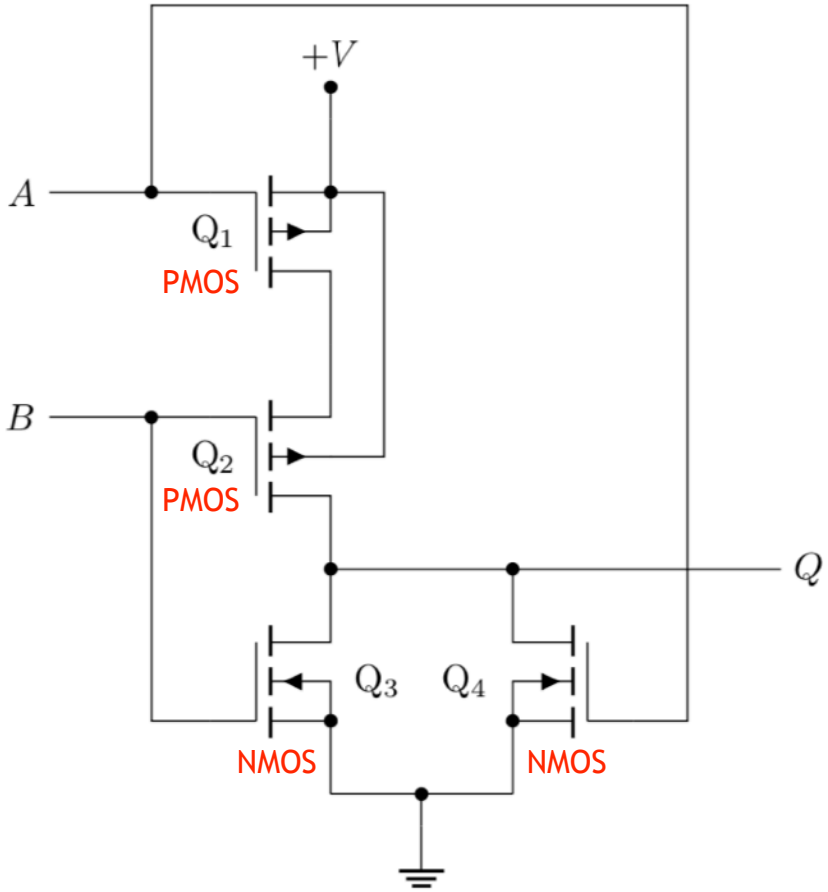

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This is a NOR = NOT OR logic gate

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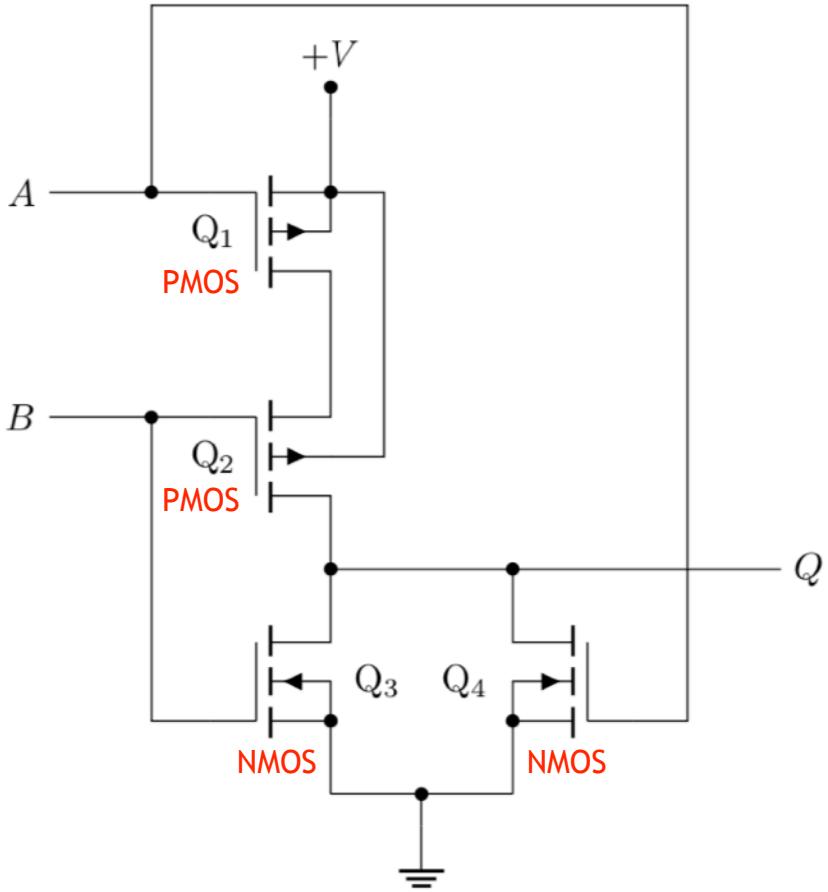

Truth table:

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1	0	0
0	1	0
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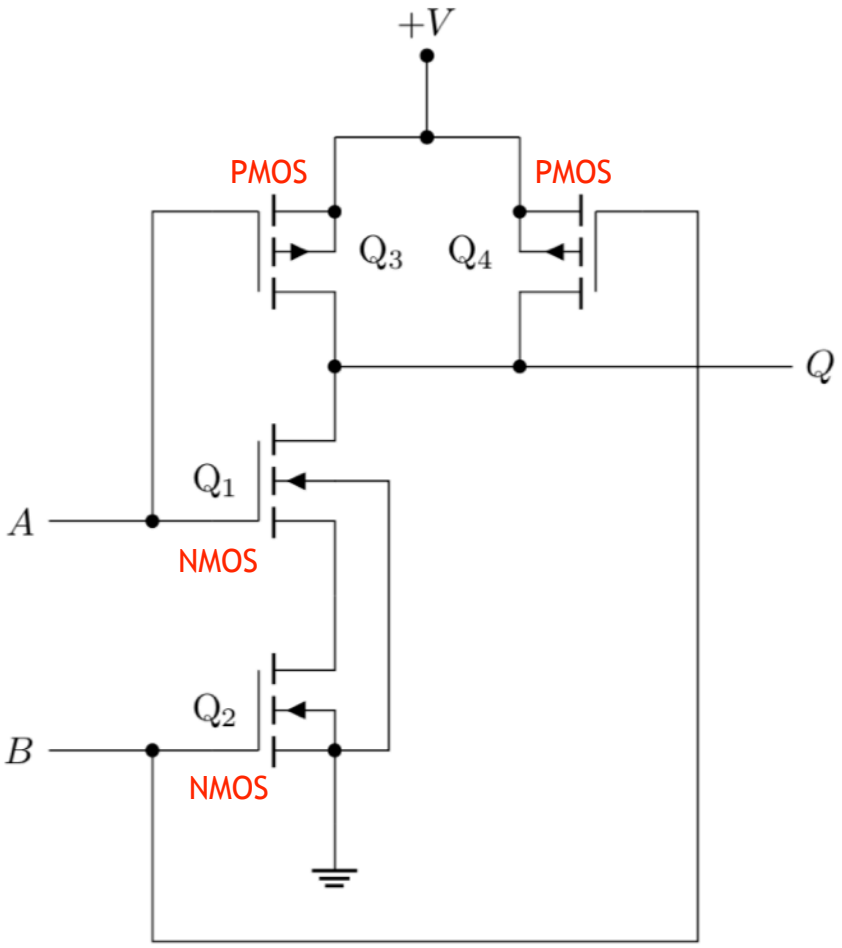

Truth table:

A	B	Q
0	0	
1	0	
0	1	
1	1	

CMOS Logic

CMOS is the workhorse of modern logic circuits