#### **PHYS127AL Lecture 8**

David Stuart, UC Santa Barbara, October 19, 2021

More transistor circuits: Ebers-Moll, current mirror, differential amplifier, FETs



### Review: Transistor rules of operation

- 1).  $V_{BE} = 0.6$  V or the transistor is off I.e.,  $V_B = V_E + 0.6$  V Once the transistor is on,  $\Delta V_B = \Delta V_E$ .
- 2).  $I_C = \beta I_B$ . And by charge conservation  $I_E = I_B + I_C$  so  $I_E \cong I_C$

3).  $V_{CE} > 0.2 V$ 

With these simple rules we can analyze most transistor circuits. With these simple rules we can analyze most dansistor encuries.  $V_{CC}$ <br>We'll add some nuance later today.





#### Review: Constant current source

We can use a transistor to pull a *constant* specified current through a load.



To get a constant 1mA flow through RL, even as  $R_L$  changes, we can set  $R_E$  to 1k and  $V<sub>E</sub>$  to 1 V.

That sets the value of  $I<sub>E</sub>$ , which is equal to I<sub>C</sub>, regardless of R<sub>L</sub>.

Choose  $R_1$  and  $R_2$  to make  $V_B = 1.6$  V. Then  $V<sub>E</sub> = 1.0 V$ .  $I<sub>E</sub> = 1$  mA.  $I_C = 1$  mA, regardless of  $R_L$ .

This works until  $V_C < V_E + 0.2$ 

*Note that there is no input signal here.*

#### Review: Constant current source

#### We can use this to pull a specified current through a load.

 $V_{CC}$  = + 5 V  $\rm V_{EE}$  $R_{\rm E}$ RL  $R_1$ 

To get a constant 1mA flow through RL, even as RL changes, we can set  $R_E$  to 1k and  $V_E$  to 1 V. That sets  $I<sub>E</sub>$  which is equal to  $I<sub>C</sub>$ , regardless of  $R<sub>L</sub>$ .

Choose the zener diode to make  $V_B = 1.6$  V. The zener reduces sensitivity to  $V_{CC}$  variations.



#### Constant current source

We can use a transistor to *pull* a *constant* specified current through a load. This is actually called a *current sink* since it pulls current from RL.



#### Constant current source

We can use a PNP transistor to *push* a *constant* specified current into a load.



Now we can switch the location of  $R_L$  and  $R_E$ . The base's bias voltage sets  $R<sub>E</sub>$  which sets  $I<sub>E</sub>$ and hence IC.

For 1 mA we could set  $R_E = 1k$  and  $V_E = 4 V$ . That requires  $V_B = 3.4$  V which we get from  $R_1 \& R_2$  choice.

 $3.4 = 5 R_2/(R_1 + R_2)$ 

### Ebers-Moll model

The simple transistor rules we have been using aren't the full picture. Two examples of features it misses.

Gain limit with  $R<sub>G</sub>=0$ .

IL is temperature dependent.



# Ebers-Moll model

Gain limit comes from intrinsic resistance in the transistor.



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We used simplified  $(0<sup>th</sup>$  and 1<sup>st</sup> order) models:

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I_C = I_s \left( e^{V_{BE}/nV_T} - 1 \right)
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2).  $I_C = \beta I_B$ . And by charge conservation  $I_E = I_B + I_C$  so  $I_E \cong I_C$ 

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A 2nd order correction incorporates effects from collector voltage differences

$$
I_{\rm C} = I_{\rm S} \left( e^{V_{\rm BE}/nV_{\rm T}} - 1 \right) \left( 1 + \frac{V_{\rm CE}}{V_{\rm AF}} \right) - I_{\rm S} \left( e^{V_{\rm BC}/nV_{\rm T}} - 1 \right) \left( 1 + \frac{V_{\rm CE}}{V_{\rm AR}} \right) - \frac{I_{\rm S}}{\beta_{\rm R}} \left( e^{V_{\rm BC}/nV_{\rm T}} - 1 \right)
$$
  

$$
I_{\rm B} = \frac{I_{\rm S}}{\beta_{\rm F}} \left( e^{V_{\rm BE}/nV_{\rm T}} - 1 \right) - \frac{I_{\rm S}}{\beta_{\rm R}} \left( e^{V_{\rm BC}/nV_{\rm T}} - 1 \right).
$$

(Ebers–Moll equations with Early correction)

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We used simplified  $(0<sup>th</sup>$  and 1<sup>st</sup> order) models: A 2nd order correction incorporates effects from collector voltage differences These are typically not important for 1).  $V_{BE} = 0.6$  V or the transistor is off  $(e^{V_{BE}/nV_T}-1)$ 0.6 V<br>
istor is on,  $\Delta V_B = \Delta V_0 \Delta V_0 \Delta V_0$ <br>
conservative and the physicists but<br>  $E \cong I_C$  and the physicists but<br>  $E \cong I_C$  and the physicists but are physicists but<br>  $E \cong I_C$  and the physicists from collector voltage I.e.,  $V_B = V_E + 0.6 V$ Once the transistor is on,  $\Delta V_B = \Delta V_{\rm B}$  $I_{\rm B} = 50 \,\mu\text{A}$ important for EE design working  $I_{\rm B} = 40 \,\mu\text{A}$ 2). I<sub>C</sub> =  $\beta$  I<sub>B</sub>.  $I_{\rm B} = 30 \,\mu A$ And by charge conservation  $I_{\rm B}$  = 20  $\mu$ A  $I_E = I_B + I_C$  so  $I_E \cong I_C$  $I_{\rm B}$  = 10  $\mu$ A 3).  $V_{CE} > 0.2 V$ (Ebers–Moll equations with Early correction)

If we try to transmit a signal a long distance, we need to worry about RF pickup because the wires act as an antenna (or capacitively couple).

We could amplify the signal before transmitting to make it large compared to any pickup. But then it becomes a powerful transmitter causing pickup on other wires nearby.



If we try to transmit a signal a long distance, we need to worry about RF pickup because the wires act as an antenna (or capacitively couple).

- We could amplify the signal before transmitting to make it large compared to any pickup. But then it becomes a powerful transmitter causing pickup on other wires nearby.
- Best to transmit signals with small signals that are immune to pickup; use low-voltage differential signals (LVDS) on twisted pairs of wires.













Analyze this by 1st calculating V<sub>A</sub>.  
\n
$$
V_A = V_{EE} + I_{EE}R_{EE}
$$
\n
$$
I_{EE} = I_{E1} + I_{E2}
$$
\n
$$
= (V_{E1} - V_A)/R_E + (V_{E2} - V_A)/R_E
$$
\n
$$
= (V_{E1} + V_{E2})/R_E - 2V_A/R_E
$$
\n
$$
V_A = V_{EE} + R_{EE}/R_E(V_{E1} + V_{E2})/R_E - 2R_{EE}V_A/R_E
$$
\n
$$
V_A = \frac{R_EV_{EE} + R_{EE}(V_{E1} + V_{E2})}{R_E + 2R_{EE}}
$$
\n
$$
\Delta V_A = (\Delta V_{E1} + \Delta V_{E2}) \frac{R_{EE}}{R_E + 2R_{EE}}
$$
\n
$$
If \Delta V_{E1} = -\Delta V_{E2} then \Delta V_A = 0
$$

This makes the right side just a common-emitter amp with  $v_{\text{out}} = (-R_C/R_E) v_2$ If  $v2 = -\Delta V_{in}/2 = -v_{in}/2$  then  $v_{out} = (R_C/R_E)v_{in}/2$ .



Differential gain = 
$$
R_C/2R_E
$$

Analyze this by  $1<sup>st</sup>$  calculating  $V_A$ .  $V_A = V_{EE} + I_{EE}R_{EE}$  $I_{EE} = I_{E1} + I_{E2}$  $= (V_{E1} - V_{A})/R_{E} + (V_{E2} - V_{A})/R_{E}$  $= (V_{E1}+V_{E2})/R_E - 2V_A/R_E$  $V_A = V_{EE} + R_{EE}/R_E (V_{E1}+V_{E2})/R_E - 2R_{EE}V_A/R_E$ VA = ———————————————— ΔVA = (ΔVE1 + ΔVE2) ————— If  $\Delta V_{E1}$  = -  $\Delta V_{E2}$  then  $\Delta V_A$  = 0  $\rm R_EV_{EE}+R_{EE}\,(V_{E1}+V_{E2})$  $R_{E}$  + 2 $R_{EE}$ REE  $R_{\rm E}$  + 2 $R_{\rm EE}$ 

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Common mode gain =  $-R_C/(R_E+2R_{EE})$ Differential gain =  $R_C/2R_E$ 

Now consider the *common mode* signal, where  $v_1 = v_2 = \overline{v} = v_{CM}$ 

That makes  $\Delta I_{E1} = \Delta I_{E2} \& \Delta I_{E} = 2\Delta I_{E1}$ 

Written with "variation notation" its  $i_{E1} = i_{E2}$  and  $i_{E} = 2i_{E1}$ 

So,  $\Delta V_A = v_A = i_{\text{EE}}R_{\text{EE}} = 2i_{\text{E1}}R_{\text{EE}}$ Now use Ohm's law to find  $i_{E1}$  as  $i_{E1} = (\nu_{E} - \nu_{A}) / R_{E}$  $= (v_{CM} - 2i_{E1}R_{EE}) / R_E$ So,  $i_{E1} = v_{CM} / (R_E + 2R_E)$ 

 $v_{\text{out}} = -i_{E1} R_C = -v_{CM} R_C / (R_E + 2R_E)$ 



Get positive gain by selecting output from  $v_2 = -v/2$ 

Don't need output from other side, but we do need the other side to get the common mode suppression.

Comment on "CM" jargon.

To maximize the CMRR  $=$  G<sub>Diff</sub>/G<sub>CM</sub> make R<sub>EE</sub> large.

A current source has infinite impedance.

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Common mode gain =  $-R_C/(R_E+2R_{EE})$  separately later. Differential gain =  $R_C/2R_E$ 

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A current source has infinite impedance.

A current mirror makes  $R_C$  large for differential signals and small for common mode.

So this circuit gives very maximal G<sub>Diff</sub> and a large common mode rejection ratio. But we no longer control the gain; we'll see how to do that

## Current limiter

Separate from having a constant current, we often want to limit  $K_{\text{max}}$ .



If  $Q_2$ 's  $V_{BE}$ <0.6 V it turns off, so no current flows through  $R_b$  and  $Q_1$  has a high  $V_b$  and  $Q_1$  is on.

If enough current flows to cause the voltage drop across  $R_s$  to go above 0.6 V,  $Q_2$  turns on and current flows through  $R_b$ . That reduces the base voltage of  $Q_1$ , lowering the current through  $Q_1$ and hence the current through  $R_s$  to turn off  $Q_2$ . This rapid on/off leads to an equilibrium at the max current of 0.6/Rs.

I.e., attempts to increase the load current beyond  $I_L = 0.6/R_s$  (either by higher V<sub>CC</sub> or lower R<sub>L</sub>) will lead to a max current of  $0.6/R_s$ .

E.g.,  $R_s = 0.6\Omega$  limits load current to 1 A.













If we wanted to drive a high current load, like a speaker, we need a low  $R_{\rm C}$  ( $X_{\rm out}$ ), and a low  $R_{\rm E}$ . So transistor dissipates a lot of power.



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Speakers are usually  $8\Omega$ , so we need a very small  $R_C$  to match.

And a very large C<sub>out</sub> for audio frequency: 20 Hz =  $1/RC = 1/8*C$  $C = 1/160 = 6mF!$ 

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Better to set the  $V_{out}$  quiescent point at ground, with a dual power supply, and DC couple the output.

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Even better to use an emitter follower as the output stage.

Amplification done in a previous stage. This just drives the speaker.

 $R<sub>E</sub>$  still needs to be small, with high power to  $V_{EE}$ .

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Fix that by making the speaker be  $R<sub>E</sub>$ Connect it only to ground But need two transistors to drive it; They push and pull current.

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Fix that by biasing each transistor by just enough  $(0.6 V)$  to turn on when Vin goes above or below zero.

A diode does that, but temperature sensitive.

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A diode does that, but temperature sensitive. So use identical copies of the push-pull transistors. (Ebers-Moll)





The NPN and PNP transistors we've discussed so far are called bi-polar junction transistors (BJT). FETs operate under a different mechanism.

![](_page_42_Figure_2.jpeg)

This is a junction FET (jFET) where a p-type region is implanted within an n-type bulk. The depletion region can be controlled by the gate. Lower  $V<sub>g</sub>$  increases the depletion.

So changing the gate voltage controls n and I. Like pinching off a hose.

![](_page_43_Figure_2.jpeg)

![](_page_44_Figure_2.jpeg)

![](_page_45_Figure_2.jpeg)

Electro-static discharge (ESD) is a risk for MOSFETs due to thin oxide.

![](_page_46_Figure_2.jpeg)

![](_page_46_Picture_3.jpeg)

![](_page_46_Picture_4.jpeg)