PHYS127AL Lecture 7

David Stuart, UC Santa Barbara

More transistor circuits: current source, PNP, bootstrapping, Ebers-Moll

Review: Transistor rules of operation

- 1). $V_{BE} = 0.6$ V or the transistor is off I.e., $V_B = V_E + 0.6$ V Once the transistor is on, $\Delta V_B = \Delta V_E$.
- 2). $I_C = \beta I_B$. And by charge conservation $I_E = I_B + I_C$ so $I_E \cong I_C$

3). $V_{CE} > 0.2 V$

With these simple rules we can analyze most transistor circuits. We'll add some nuance later today.

Review: Emitter follower

This transistor circuit has the output "follow" the input, with a 0.6 V drop. $X_{in} = \beta R_E$

Review: Emitter follower

We can remove the clipping at $0 \vee y$ setting V_{EE} to a negative supply. $X_{in} = \beta R_E$

Output clips at V_{CC} and 0.6 V above V_{EE} .

Review: Common-emitter amplifier

We can use the current amplification of the transistor to get voltage amplification. $\Delta V_{\rm E} = \Delta V_{\rm B} = \Delta V_{\rm in}$

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Suppose I want a max input swing of ± 0.1 V Set V_E to vary from -4.8 to -5.0 V, i.e., DC set point for V_E is -4.9 V. DC set point for V_{in} is -4.3 V. These are called the *quiescent* values, meaning "when quiet, ie without signal".

Choose R_1 and R_2 to be a voltage divider setting V_{in} at -4.3 V.

 $V_{in} = V_{EE} + (V_{CC} - V_{EE}) * R_2 / (R_1 + R_2)$ $-4.3 = -5 + 10*1k/(1k+R_2)$ $R_1 = 13k$ and $R_2 = 1k$ Or I could use $R_1 = 130k$ and $R_2 = 10k$ Which choice is better?

Apply an input bias that puts the emitter close to V_{EE} , within a ΔV that defines the max input swing.

Suppose I want a max input swing of ± 0.1 V Set quiescent points: V_E =-4.9 V & V_{in} =-4.3 V. $R_1 = 130k$ and $R_2 = 10k$

To avoid having this stage yank the output of the previous stage to a different voltage, we *decouple* the input from this "DC bias voltage" with a "decoupling capacitor", Cin.

RinCin make a high-pass filter letting the signal through and blocking the DC offsets. What is R_{in}?

Apply an input bias that puts the emitter close to V_{EE} , within a ΔV that defines the max input swing.

Input impedance is all paths from input to a fixed voltage (V_{CC} , V_{EE} , or Gnd).

 $R_{in} = R_1 \parallel R_2 \parallel \beta R_E \cong 130k \parallel 10k \parallel \beta R_E \cong R_2$.

High-pass filter should have f_{3dB} signal frequency range. For audio signals, that is 20 Hz, so

 $20 = 1/2\pi(10k)C$

 $C \approx 1/6*120*10k \approx 1/1k*10k = 0.1 \mu F$

Now we need to pick R_E and R_C

The ratio of R_E and R_C is set by the desired gain, and avoiding output clipping.

Choose gain = 10, and max V_{in} = 0.1 V. That means V_{out} swings by ± 1 V. Then quiescent point for V_{out} to be at least 1 V away from V_{CC} and V_{E} . But,

 $V_{\text{out}} = V_{\text{CC}} - V_{\text{E}}(R_{\text{C}}/R_{\text{E}}) + V_{\text{EE}}(R_{\text{C}}/R_{\text{E}})$ only depends on the gain ratio.

$$
V_{\text{out}} = 5 - (-4.9 * 10) - 5 * 10
$$

= 4

That works, but just barely.

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The challenge here is that R_E affects both the gain and the quiescent V_{out} . A small R_E gives big gain but large I_E which affects quiescent V_{out} .

We want a large R_E for setting quiescent voltages and a small RE for setting gain.

The challenge here is that R_E affects both the gain and the quiescent V_{out} . A small R_E gives big gain but large I_E which affects quiescent V_{out} .

We want a large R_E for setting \underline{DC} quiescent voltages and a small R_E for setting AC gain.

Finally, what can we do about the 1 V quiescent offset on V_{out} ?

This also works if V_{EE} is ground. We just choose quiescent points. In fact with V_{EE}=Gnd, we *must* have input biasing.

Some checks of understanding.

 V_{CC} = + 5 V $\rm V_{EE}$ R_E Vout V_{in} o-RC $R₂$ R_1 C_{in} C_g $R_{\rm G}$ Cout

Without DC biasing, what would limit the signal?

What is the output impedance of this circuit?

With $V_{EE} = Gnd$, about where should you put the quiescent V_{out} ? Where is the quiescent V_{in} ? In general, how do you maximize the *dynamic range*?

What would happen if you set $R_G = 0$?

Common-emitter amplifier operation

The transistor is changing the voltage dropped across it to satisfy the rules of operation.

Increase in V_{in} causes increase in V_{E} That causes an increase in I_E That causes a decrease in V_C The voltage across the transistor, V_{CE} , goes down to compensate.

Review: Common-emitter amp AC gain control

We separated the determination of quiescent points from determination of gain with a gain resistor that only matters for signal because of CG.

$$
Gain = \Delta V_{out} / \Delta V_{in} = - R_{C} / (R_{E} \parallel (R_{G} + C_{G}))
$$

Gain = - R_{C} / R_{G}

 R_E can be chosen to set V_{out} quiescent point. It can be large, and so can R_C.

RG then is chosen to set the gain, it can vary without altering quiescent points, and it needn't be too small.

Common-emitter amp input impedance

What is the input impedance of the common-emitter amp?

Follow all paths to fixed voltages.

$$
X_{in} = C_{in} + \{R_1 \parallel R_2 \parallel \beta(R_E \parallel [R_G + C_G])\}
$$

\n
$$
\cong 0 + \{R_1 \parallel R_2 \parallel \beta(R_E \parallel [R_G + 0])\}
$$

\n
$$
\cong 0 + \{R_1 \parallel R_2 \parallel \beta R_G\}
$$

\n
$$
\cong R_2 \parallel \beta R_G
$$

\n
$$
\text{To bias } V_E \text{ close to } V_{EE}
$$

Can make βRG reasonably large. What about R_2 ?

We can make the bias network have very large impedance with a trick called bootstrapping. It uses the same signal specific impedance trick as C_G does.

Bootstrapping

Add capacitive feedback from V_E to V_B .

Now the input impedance is $X_{in} = C_{in} + \beta(R_E \parallel [R_G + C_G] \parallel \{C_b + R_1 \parallel R_2\}) \parallel$ $[R_3+(R_1 \parallel R_2 \parallel {C_B+R_E \parallel [R_G+C_G]})]$ $\cong \beta(R_E \parallel R_G \parallel R_1 \parallel R_2) \parallel$ $[R_3 + (R_1 \parallel R_2 \parallel R_E \parallel R_G)]$ $\cong R_3 + (R_1 \parallel R_2 \parallel R_E \parallel R_G)$

The bootstrapping trick is to make R_3 go to infinity <u>for signal</u>.

This works because $X_{C_b}=0$ for signal and $\Delta V_B = \Delta V_E$ for signal.

Bootstrapping

Add capacitive feedback from V_E to V_B .

The input impedance is $X_{in} \cong R_3 + (R_1 \parallel R_2 \parallel R_E \parallel R_G)$

Imagine a small signal $v_{in} = \Delta V_{in}$. It passes through C_{in} and also through the transistor because $\Delta V_B = \Delta V_E$.

 $v_{\text{in}} = v_{\text{B}} = v_{\text{E}} = v_{\text{3}}$

This means a small signal moves the top and bottom of R₃ the same, $v_B = v_3$.

The ΔV across R₃ is 0. So no signal current has to flow through R_3 into R_1 and R₂. The impedance of R₃ $\rightarrow \infty$ making R_1 and R_2 unimportant for X_{in} .

Separate DC and AC response.

We can use a transistor to pull a *constant* specified current through a load.

To get a constant 1mA flow through RL, even as R_L changes, we can set R_E to 1k and V_E to 1 V.

That sets the value of I_E , which is equal to IC, regardless of RL.

Choose R_1 and R_2 to make $V_B = 1.6$ V. Then $V_E = 1.0 V$. $I_E = 1$ mA. $I_C = 1$ mA, regardless of R_L .

This works until $V_C < V_E + 0.2$

Note that there is no input signal here.

We can use this to pull a specified current through a load.

To get a constant 1mA flow through RL, even as RL changes, we can set R_E to 1k and V_E to 1 V. That sets I_E which is equal to I_C , regardless of R_L .

Choose the zener diode to make $V_B = 1.6$ V. The zener reduces sensitivity to V_{CC} variations.

We can use a transistor to *pull* a *constant* specified current through a load. This is actually called a *current sink* since it pulls current from RL.

We can use a PNP transistor to *push* a *constant* specified current into a load.

Now we can switch the location of R_L and R_E . The base's bias voltage sets R_E which sets I_E and hence IC.

For 1 mA we could set $R_E = 1k$ and $V_E = 4 V$. That requires $V_B = 3.4$ V which we get from $R_1 \& R_2$ choice.

 $3.4 = 5 R_2/(R_1 + R_2)$

Current limiter

Separate from having a constant current, we often want to limit K_{max} .

If Q_2 's V_{BE} <0.6 V it turns off, so no current flows through R_b and Q_1 has a high V_b and Q_1 is on.

If enough current flows to cause the voltage drop across R_s to go above 0.6 V, Q_2 turns on and current flows through R_b . That reduces the base voltage of Q_1 , lowering the current through Q_1 and hence the current through R_s to turn off Q_2 . This rapid on/off leads to an equilibrium at the max current of 0.6/Rs.

I.e., attempts to increase the load current beyond $I_L = 0.6/R_s$ (either by higher V_{CC} or lower R_L) will lead to a max current of $0.6/R_s$.

E.g., $R_s = 0.6\Omega$ limits load current to 1 A.

Ebers-Moll model

The simple transistor rules we have been using aren't the full picture. Two examples of features it misses.

Gain limit with $R_G=0$.

IL is temperature dependent.

Ebers-Moll model

Gain limit comes from intrinsic resistance in the transistor.

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Ebers-Moll model & transconductance

This illustrates something called transconductance, which is like gain but unit-full. Gain = $\Delta V_{\text{out}} / \Delta V_{\text{in}}$ is unitless. But really, changing V_{in} changes V_{BE} . That changes Ic through the Ebers-Moll relation. $\mathsf{V}_{\rm BE}$

So the transistor's "gain" is really $g_m = \Delta I_C / \Delta V_{in}$.

This is called transconductance because conductance is 1/resistance, and the sub-m is short for mho, which is opposite of ohm.

The R_C and R_E used in a common emitter amplifier convert that ΔI_C back into a ΔV_{out} .

Ebers-Moll model & transconductance

$$
I = I_{\rm s} \left(e^{V/nV_{\rm T}} - 1 \right) \approx I_{\rm s} e^{V_{\rm BE}/nV_{\rm T}}
$$

Strong function of V_{BE} , e.g., ΔV_{BE} = 18 mV doubles I_C. ΔV_{BE} = 60 mV increases I_C by x10.

We can see where r_e comes from by calculating dI/dV .

$$
1/r_e = dI/dV = (1/nV_T) I_s e^{VBE/nV_T} = I/nV_T
$$

 $r_e = nV_T/I = 25$ mV/I = 25 Ω / I[mA] at room temperature

Ebers-Moll model & temperature effects

$$
I = I_{\rm s} \left(e^{V/nV_{\rm T}} - 1 \right) \cong I_{\rm s} \, e^{V_{\rm BE}/nV_{\rm T}} \cong I_{\rm s} \, e^{V_{\rm BE} q/k_{\rm B}T}
$$

We can see the effect of temperature on our current mirror.

Set $V_B \cong 5.6$, so $V_E = 5.0$ V and $I_E = 1$ mA. If temperature increases, $I_C = I_E$ reduces. That reduces V_E which increases V_{BE} which increases I_C. So we have "negative feedback" holding the circuit at an equilibrium behavior, insensitive to temperature. But, I_S is also temperature dependent, with opposite and stronger dependence, $\sim 9\%/^{\circ}C$. So we need to build in more negative feedback.

Current mirror for temperature stability

$$
I = I_{\rm s} \left(e^{V/nV_{\rm T}} - 1 \right) \cong I_{\rm s} \, e^{V_{\rm BE}/nV_{\rm T}} \cong I_{\rm s} \, e^{V_{\rm BE} q/k_{\rm B}T}
$$

Set (program) Ip on left side.

Current mirror for temperature stability

$$
I = I_{\rm s} \left(e^{V/nV_{\rm T}} - 1 \right) \cong I_{\rm s} e^{V_{\rm BE}/nV_{\rm T}} \cong I_{\rm s} e^{V_{\rm BE}q/k_{\rm B}T}
$$

Set (program) In on left side.
\n
$$
V_B = V_{CC} - 0.6 = V_C
$$

\n $I_p = V_C/R_p$
\n $I_{load} = I_p$ because V_{BE} for Q_2 is the same as V_{BE} for Q_1 .

Current mirror for temperature stability

$$
I = I_{\rm s} \left(e^{V/nV_{\rm T}} - 1 \right) \cong I_{\rm s} \, e^{V_{\rm BE}/nV_{\rm T}} \cong I_{\rm s} \, e^{V_{\rm BE} q/k_{\rm B}T}
$$

Set (program) Ip on left side. $V_B = V_{CC} - 0.6 = V_C$ $I_p = V_C/R_p$ $I_{load} = I_p$ because V_{BE} for Q_2 is the same as V_{BE} for Q_1 .

Use matched transistors:

- same doping concentrations means same I_S, and I_S(T);
- same substrate means same temperature.

Then they also have the same Ebers-Moll relation.

If some ΔT causes I_p to increase, then R_p pushes V_{BE} up to reduce I_p . Same change on both sides.

- If we try to transmit a signal a long distance, we need to worry about RF pickup because the wires act as an antenna.
- We could amplify the signal before transmitting to make it large compared to any pickup. But then it becomes a powerful transmitter causing pickup on other wires nearby.

- If we try to transmit a signal a long distance, we need to worry about RF pickup because the wires act as an antenna.
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- Best to transmit signals with small signals that are immune to pickup; use low-voltage differential signals (LVDS) on twisted pairs of wires.

Analyze this by 1st calculating V_A.
\n
$$
V_A = V_{EE} + I_{EE}R_{EE}
$$
\n
$$
I_{EE} = I_{E1} + I_{E2}
$$
\n
$$
= (V_{E1} - V_A)/R_E + (V_{E2} - V_A)/R_E
$$
\n
$$
= (V_{E1} + V_{E2})/R_E - 2V_A/R_E
$$
\n
$$
V_A = V_{EE} + R_{EE}/R_E(V_{E1} + V_{E2})/R_E - 2R_{EE}V_A/R_E
$$
\n
$$
V_A = \frac{R_EV_{EE} + R_{EE}(V_{E1} + V_{E2})}{R_E + 2R_{EE}}
$$
\n
$$
\Delta V_A = (\Delta V_{E1} + \Delta V_{E2}) \frac{R_{EE}}{R_E + 2R_{EE}}
$$
\n
$$
If \Delta V_{E1} = -\Delta V_{E2} then \Delta V_A = 0
$$

This makes the right side just a common-emitter amp with $v_{\text{out}} = (-R_C/R_E) v_2$ If $v2 = -\Delta V_{in}/2 = -v_{in}/2$ then $v_{out} = (R_C/R_E)v_{in}$.

Common mode gain = $-R_C/(R_E+2R_{EE})$ Differential gain = $-R_C/2R_E$

Now consider the *common mode* signal, where $v_1 = v_2 = \overline{v} = v_{CM}$

That makes $\Delta I_{E1} = \Delta I_{E2} \& \Delta I_{E} = 2\Delta I_{E1}$

Written with "variation notation" its $i_{E1} = i_{E2}$ and $i_{E} = 2i_{E1}$

So, $\Delta V_A = v_A = i_{\text{EE}}R_{\text{EE}} = 2i_{\text{E1}}R_{\text{EE}}$ Now use Ohm's law to find *i*E1 as $i_{E1} = (v_E - v_A)/R_E$ $= (v_{CM} - 2i_{E1}R_{EE})/R_E$ So, $i_{E1} = v_{CM}/(R_{E} + 2R_{EE})$

 $v_{\text{out}} = -i_{E1}$ $R_C = -v_{CM} R_C/(R_E + 2R_{EE})$